NANO SPIDER (ORG4400)
GPS RECEIVER MODULE
DATASHEET

OriginGPS.com
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1. SCOPE
This document describes the features and specifications of Nano Spider ORG4400 GPS receiver module.

2. DISCLAIMER
All trademarks are properties of their respective owners. Performance characteristics listed in this document do not constitute a warranty or guarantee of product performance. OriginGPS assumes no liability or responsibility for any claims or damages arising out of the use of this document, or from the use of integrated circuits based on this document. OriginGPS assumes no liability or responsibility for unintentional inaccuracies or omissions in this document. OriginGPS reserves the right to make changes in its products, specifications and other information at any time without notice. OriginGPS reserves the right to conduct, from time to time, and at its sole discretion, firmware upgrades. As long as those FW improvements have no material change on end customers, PCN may not be issued. OriginGPS navigation products are not recommended to use in life saving or life sustaining applications.

3. SAFETY INFORMATION
Improper handling and use can cause permanent damage to the product.

4. ESD SENSITIVITY
This product is ESD sensitive device and must be handled with care.

5. CONTACT INFORMATION
Support - support@origingps.com or Online Form
Marketing and sales - marketing@origingps.com
Web – www.origingps.com

6. RELATED DOCUMENTATION

<table>
<thead>
<tr>
<th>No</th>
<th>DOCUMENT NAME</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Spider and Hornet - NMEA Protocol Reference Manual</td>
</tr>
<tr>
<td>3</td>
<td>Spider and Hornet - Low Power Modes Application Note</td>
</tr>
<tr>
<td>4</td>
<td>SirFLive FAQ</td>
</tr>
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TABLE 1 – RELATED DOCUMENTATION
### 7. REVISION HISTORY

<table>
<thead>
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<th>REVISION</th>
<th>DATE</th>
<th>CHANGE DESCRIPTION</th>
</tr>
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<tr>
<td>0.0</td>
<td>October 21, 2014</td>
<td>Draft</td>
</tr>
<tr>
<td>1.0</td>
<td>March 10, 2015</td>
<td>Release</td>
</tr>
<tr>
<td>1.1</td>
<td>October 18, 2015</td>
<td>Figures 9,10 update</td>
</tr>
<tr>
<td>1.2</td>
<td>February 2, 2016</td>
<td>Figure 9 - LNA P/N update</td>
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<tr>
<td>1.3</td>
<td>June 5, 2016</td>
<td>Power Modes update</td>
</tr>
<tr>
<td>1.4</td>
<td>July 4, 2016</td>
<td>Default interface update - UART</td>
</tr>
<tr>
<td>1.5</td>
<td>August 13, 2017</td>
<td>Footprint – dimensions in mm update</td>
</tr>
<tr>
<td>1.6</td>
<td>October 1, 2017</td>
<td>Related Documentation update, Default interface update, removal of I2C slave mode</td>
</tr>
<tr>
<td>1.7</td>
<td>February 14, 2018</td>
<td>Section 18.4 Antenna Switch removal</td>
</tr>
<tr>
<td>1.8</td>
<td>23-Apr-18</td>
<td>Update Absolute Maximum Rating</td>
</tr>
<tr>
<td>1.9</td>
<td>June 4 2018</td>
<td>Update active / passive antennas</td>
</tr>
<tr>
<td>2.0</td>
<td>June 25, 2018</td>
<td>Update I2C info</td>
</tr>
<tr>
<td>2.1</td>
<td>Feb. 10, 2020</td>
<td>Update Pad Assignment</td>
</tr>
<tr>
<td>2.2</td>
<td>June 20, 2020</td>
<td>Update Assembly</td>
</tr>
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</table>

TABLE 2 – REVISION HISTORY
8. GLOSSARY

A-GPS Assisted GPS
ABP™ Almanac Based Position
AC Alternating Current
ADC Analog to Digital Converter
AGC Automatic Gain Control
APM™ Adaptive Power Management
ATP™ Adaptive Trickle Power
BBRAM Battery Backed-up RAM
BE Broadcast Ephemeris
BPF Band Pass Filter
C/N0 Carrier to Noise density ratio [dB-Hz]
CDM Charged Device Model
CE European Community conformity mark
CEP Circular Error Probability
CGEE™ Client Generated Extended Ephemeris
CMOS Complementary Metal-Oxide Semiconductor
CPU Central Processing Unit
CTS Clear-To-Send
CW Continuous Wave
DC Direct Current
DOP Dilution Of Precision
DR Dead Reckoning
DSP Digital Signal Processor
ECEF Earth Centred Earth Fixed
ECHA European Chemical Agency
EE Extended Ephemeris
EGNOS European Geostationary Navigation Overlay Service
EIA Electronic Industries Alliance
EMC Electro-Magnetic Compatibility
EMI Electro-Magnetic Interference
ENIG Electroless Nickel Immersion Gold
ESD Electro-Static Discharge
ESR Equivalent Series Resistance
EU European Union
EVB Evaluation Board
EVK Evaluation Kit
FCC Federal Communications Commission
FSM Finite State Machine
GAGAN GPS Aided Geo-Augmented Navigation
GNSS Global Navigation Satellite System
GPIO General Purpose Input or Output
GPS Global Positioning System
HBM Human Body Model
HDOP Horizontal Dilution Of Precision
I²C Inter-Integrated Circuit
I/O Input or Output
IC Integrated Circuit
ICD Interface Control Document
IF Intermediate Frequency
ISO International Organization for Standardization
9. ABOUT SPIDER FAMILY
OriginGPS GNSS receiver modules have been designed to address markets where size, weight, stand-alone operation, highest level of integration, power consumption and design flexibility - all are very important.
OriginGPS' Spider family breaks size barrier, offering the industry’s smallest fully-integrated, highly-sensitive GPS and GNSS modules.
Spider family features OriginGPS' proprietary NFZ™ technology for high sensitivity and noise immunity even under marginal signal condition, commonly found in urban canyons, under dense foliage or when the receiver’s position in space rapidly changes.
Spider family enables the shortest TTM (Time-To-Market) with minimal design risks.
Just connect an antenna and power supply on a 2-layer PCB.

10. ABOUT NANO SPIDER MODULE
Nano Spider is a complete SiP featuring LGA SMT footprint designed to commit unique integration features for high volume cost sensitive applications.
Designed to support ultra-compact applications such as smart watches, wearable devices, trackers and digital cameras, Nano Spider ORG4400 module is a miniature multi-channel GPS with SBAS, QZSS and other regional overlay systems receiver that continuously tracks all satellites in view, providing real-time positioning data in industry’s standard NMEA format.
Nano Spider ORG4400 module offers superior sensitivity and outstanding performance, achieving rapid TTFF in less than one second, accuracy of approximately two meters, and tracking sensitivity of -163dBm.
Sized only 4.1mm x 4.1mm Nano Spider ORG4400 module is industry’s small sized, record breaking solution.
ORG4400 module integrates LNA, SAW filter, TCXO, RTC crystal shield with market-leading SiRFstarIV™ GPS SoC.
Nano Spider ORG4400 module is introducing industry’s lowest energy per fix ratio, unparalleled accuracy and extremely fast fixes even under challenging signal conditions, such as in built-up urban areas, dense foliage or even indoor.
Integrated GPS SoC incorporating high-performance microprocessor and sophisticated firmware keeps positioning payload off the host, allowing integration in embedded solutions with low computing resources.
Innovative architecture can detect changes in context, temperature, and satellite signals to achieve a state of near continuous availability by maintaining and opportunistically updating its internal fine time, frequency, and satellite ephemeris data while consuming mere microwatts of battery power.

11. ABOUT ORIGINGPS
OriginGPS is a world leading designer, manufacturer and supplier of miniature positioning modules, antenna modules and antenna solutions.
OriginGPS modules introduce unparalleled sensitivity and noise immunity by incorporating Noise Free Zone system (NFZ™) proprietary technology for faster position fix and navigation stability even under challenging satellite signal conditions.
Founded in 2006, OriginGPS is specializing in development of unique technologies that miniaturize RF modules, thereby addressing the market need for smaller wireless solutions.
12. DESCRIPTION

12.1. FEATURES

- Autonomous operation
- OriginGPS Noise Free Zone System (NFZ™) technology
- Fully integrating:
  - LNA, SAW Filter, TCXO, RTC Crystal, GPS SoC, Power Management Unit
- Active or Passive antenna support
- GPS L1 1575.42 frequency, C/A code
- SBAS (WAAS, EGNOS, MSAS) and QZSS support
- 48 channels
- Ultra-high Sensitivity down to -163dBm enabling Indoor Tracking
- TTFF of < 1s in 50% of trials under Hot Start conditions
- Low Power Consumption of < 9mW in ATP™ mode
- High Accuracy of < 2.5m in 50% of trials
- High update rate of 5Hz, 1Hz by default
- Autonomous A-GPS by Client Generated Extended Ephemeris (CGEE™) for non-networked devices
- Predictive A-GPS by Server Generated Extended Ephemeris (SGEE™) for connected devices
- Ephemeris Push™ for storing and loading broadcast ephemeris
- Host controlled power saving mode
- Self-managed low power modes - ATP™, PTF™ and APM™
- Almanac Based Positioning (ABP™)
- Multipath and cross-correlation mitigation
- Active Jammer Detector and Remover
- Fast Time Synchronization for rapid single satellite time solution
- ARM7® microprocessor system
- Selectable UART, SPI or I²C host interface
- NMEA protocol by default, switchable into One Socket Protocol (OSP™)
- Programmable baud rate and messages rate
- 1PPS output
- Antenna input DC blocked and matched 50Ω
- Single voltage supply
- Ultra-small LGA footprint of 4.1mm x 4.1mm
- Surface Mount Device (SMD)
- Optimized for automatic assembly and reflow processes
- Operating from -40°C to +85°C
- FCC, CE, VCCI certified
- RoHS II/REACH compliant
12.2. ARCHITECTURE

**SAW Filter**
Band-Pass SAW filter eliminates out-of-band signals that may interfere to GPS reception. SAW filter is optimized for low insertion-loss in GPS band and low return-loss outside it.

**LNA**
Integrated LNA amplifies GPS signals to meet RF down converter input threshold. Noise Figure optimized design was implemented to provide maximum sensitivity.

**TCXO**
Highly stable 16.369 MHz oscillator controls the down conversion process in RF block of the GPS SoC. Characteristics of this component are important factors for higher sensitivity, shorter TTFF and better navigation stability.

**RTC crystal**
Tuning fork 32.768 KHz quartz crystal with very tight specifications is necessary for maintaining Hot Start and Warm Start capabilities of the module.
**SiRFstarIV™ GSD4e GPS SoC**

SiRFstarIV™ GSD4e is full SoC built on a low-power RF CMOS single-die, incorporating GPS RF, baseband, integrated navigation solution software and ARM® processor.

*FIGURE 2 – SiRFstarIV™ GSD4e GPS SoC BLOCK DIAGRAM*

SiRFstarIV™ GSD4e SoC includes the following units:

- **GPS radio subsystem** containing LNA, harmonic-reject double balanced mixer, fractional-N synthesizer, integrated self-calibrating filters, IF VGA with AGC, high-sample rate ADCs with adaptive dynamic range.

- Measurement subsystem including DSP core for GPS signals acquisition and tracking, interference scanner and detector, wideband and narrowband interference removers, multipath and cross-correlation detectors, dedicated DSP code ROM and DSP cache RAM. Measurement subsystem interfaces GPS radio subsystem.

- **Navigation subsystem** comprising ARM7® microprocessor system for position, velocity and time solution, program ROM, data RAM, cache and patch RAM, host interface UART, SPI and I2C drivers. Navigation subsystem interfaces measurement subsystem.

- **Auxiliary subsystem** containing RTC block and health monitor, temperature sensor for reference clock compensation, battery-backed SRAM for satellite data storage, voltage supervisor with POR, PLL controller, GPIO controller, 48-bit RTC timer and alarms, CPU watchdog monitor. Auxiliary subsystem interfaces navigation subsystem, PLL and PMU subsystems.

- **PMU subsystem** containing voltage regulators for RF and baseband domains.
13. ELECTRICAL SPECIFICATIONS

13.1. ABSOLUTE MAXIMUM RATINGS

Stresses exceeding Absolute Maximum Ratings may damage the device.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>VCC</td>
<td>-0.30</td>
<td>+2.20</td>
<td>V</td>
</tr>
<tr>
<td>Power Supply Current(^1)</td>
<td>ICC</td>
<td>100</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>I/O Voltage</td>
<td>V(_{IO})</td>
<td>-0.30</td>
<td>+3.65</td>
<td>V</td>
</tr>
<tr>
<td>I/O Source/Sink Current</td>
<td>I(_{IO})</td>
<td>-4</td>
<td>+4</td>
<td>mA</td>
</tr>
<tr>
<td>ESD Rating</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O pads</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HBM(^2) method</td>
<td>(V_{IO(ESD)})</td>
<td>-2000</td>
<td>+2000</td>
<td>V</td>
</tr>
<tr>
<td>CDM(^3) method</td>
<td></td>
<td>-400</td>
<td>+400</td>
<td>V</td>
</tr>
<tr>
<td>RF input pad</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HBM(^2) method</td>
<td>(V_{RF(ESD)})</td>
<td>-500</td>
<td>+500</td>
<td>V</td>
</tr>
<tr>
<td>CDM(^3) method</td>
<td></td>
<td>-100</td>
<td>+100</td>
<td>V</td>
</tr>
<tr>
<td>RF Input Power</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(f_N = 1560MHz \pm 1590MHz)</td>
<td>(P_{RF})</td>
<td>+10</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>(f_N &lt; 1560MHz, &gt; 1590MHz)</td>
<td></td>
<td>+30</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>(P_D)</td>
<td>220</td>
<td></td>
<td>mW</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>(T_{AMB})</td>
<td>-45</td>
<td>+90</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>(T_{ST})</td>
<td>-55</td>
<td>+150</td>
<td>°C</td>
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<tr>
<td>Lead Temperature(^4)</td>
<td>(T_{LEAD})</td>
<td></td>
<td>+260</td>
<td>°C</td>
</tr>
</tbody>
</table>

TABLE 3 – ABSOLUTE MAXIMUM RATINGS

Notes:
1. Inrush current of up to 100mA for about 20µs duration.
2. Human Body Model (HBM) contact discharge per EIA/JEDEC JESD22-A114D.
3. Charged Device Model (CDM) contact discharge per EIA/JEDEC JESD22-C101.
4. Lead temperature at 1mm from case for 10s duration.
13.2. RECOMMENDED OPERATING CONDITIONS

Exposure to stresses above the Recommended Operating Conditions may affect device reliability.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MODE / PAD</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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<tr>
<td>Power supply voltage</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>Acquisition</td>
<td>+1.71</td>
<td>+1.80</td>
<td>+1.89</td>
<td>V</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Tracking</td>
<td>5</td>
<td>33</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Power Supply Current&lt;sup&gt;1&lt;/sup&gt;</td>
<td>I&lt;sub&gt;CC&lt;/sub&gt;</td>
<td></td>
<td>ATP™ Tracking&lt;sup&gt;2&lt;/sup&gt;</td>
<td>5</td>
<td></td>
<td>5</td>
<td>mA</td>
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<td></td>
<td></td>
<td></td>
<td>CPU only&lt;sup&gt;3&lt;/sup&gt;</td>
<td>14</td>
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<td></td>
<td>mA</td>
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<td></td>
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<td>Standby&lt;sup&gt;5&lt;/sup&gt;</td>
<td>90</td>
<td></td>
<td>90</td>
<td>µA</td>
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<td></td>
<td></td>
<td></td>
<td>PTF™&lt;sup&gt;4&lt;/sup&gt;</td>
<td>400</td>
<td></td>
<td></td>
<td>µA</td>
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<td></td>
<td></td>
<td>Hibernate</td>
<td>9</td>
<td>14</td>
<td>15</td>
<td>µA</td>
</tr>
<tr>
<td>Input Voltage Low State</td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>GPIO</td>
<td></td>
<td>-0.40</td>
<td></td>
<td>0.45</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage High State</td>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>0.70·V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td></td>
<td>+3.60</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage Low State</td>
<td>V&lt;sub&gt;OL&lt;/sub&gt;</td>
<td></td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 2mA</td>
<td></td>
<td>+0.40</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage High State</td>
<td>V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td></td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = -2mA</td>
<td>0.75·V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Internal Pull-up Resistor</td>
<td>R&lt;sub&gt;PU&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>50</td>
<td>86</td>
<td>157</td>
<td>kΩ</td>
</tr>
<tr>
<td>Internal Pull-down Resistor</td>
<td>R&lt;sub&gt;PD&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>51</td>
<td>91</td>
<td>180</td>
<td>kΩ</td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>I&lt;sub&gt;IN&lt;/sub&gt;(leak)</td>
<td>GPIO</td>
<td></td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; ≈ 1.8V or 0V</td>
<td>-10</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>I&lt;sub&gt;OUT&lt;/sub&gt;(leak)</td>
<td>RF Input</td>
<td></td>
<td>V&lt;sub&gt;OUT&lt;/sub&gt; ≈ 1.8V or 0V</td>
<td>-10</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>Z&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>RF Input</td>
<td></td>
<td>f&lt;sub&gt;IN&lt;/sub&gt; = 1575.5MHz</td>
<td>50</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>R&lt;sub&gt;LIN&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>-8</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Input Power Range</td>
<td>P&lt;sub&gt;IN&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>-165</td>
<td>-110</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Input Frequency Range</td>
<td>f&lt;sub&gt;IN&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>1575.42</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Operating Temperature&lt;sup&gt;6&lt;/sup&gt;</td>
<td>T&lt;sub&gt;AMB&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>-40</td>
<td>25</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>T&lt;sub&gt;ST&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>-55</td>
<td>25</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Relative Humidity&lt;sup&gt;7&lt;/sup&gt;</td>
<td>RH</td>
<td></td>
<td></td>
<td>T&lt;sub&gt;AMB&lt;/sub&gt;</td>
<td>5</td>
<td>95</td>
<td>%</td>
</tr>
</tbody>
</table>

**Notes:**
1. Typical I<sub>CC</sub> values are under signal conditions of -130dBm and ambient temperature of +25°C.
2. ATP™ mode 200:1 (200ms on-time, 1s period).
3. Transitional states of ATP™ power saving mode.
4. PTF™ mode 30:30 (30s max. on-time – 18s typical, 30m period).
5. Longest TTFF is expected while operating below -30°C to -40°C.
6. Relative Humidity is within Operating Temperature range.

**TABLE 4 – RECOMMENDED OPERATING CONDITIONS**
14. PERFORMANCE

14.1. ACQUISITION TIME

TTFF (Time To First Fix) – is the period of time from the module’s power-up till position estimation.

14.1.1. HOT START

Hot Start results either from a software reset after a period of continuous navigation or a return from a short idle period that was preceded by a period of continuous navigation.

During Hot Start all critical data (position, velocity, time, and satellite ephemeris) is valid to the specified accuracy and available in RAM.

14.1.2. SIGNAL REACQUISITION

Reacquisition follows temporary blocking of GPS signals.

Typical reacquisition scenario includes driving through tunnel.

14.1.3. AIDED START

Aided Start is a method of effectively reducing TTFF by providing valid satellite ephemeris data.

Aiding can be implemented using Ephemeris Push™, CGEE™ or SGEE™.

14.1.4. WARM START

Warm Start typically results from user-supplied position and time initialization data or continuous RTC operation with an accurate last known position available in RAM.

In this state position and time data are present and valid, but satellite ephemeris data validity has expired.

14.1.5. COLD START

Cold Start occurs when satellite ephemeris data, position and time data are unknown.

Typical Cold Start scenario includes first power application.

<table>
<thead>
<tr>
<th>OPERATION</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hot Start</td>
<td>&lt; 1</td>
<td>s</td>
</tr>
<tr>
<td>Signal Reacquisition</td>
<td>&lt; 1</td>
<td>s</td>
</tr>
<tr>
<td>Aided Start</td>
<td>&lt; 10</td>
<td>s</td>
</tr>
<tr>
<td>Warm Start</td>
<td>&lt; 32</td>
<td>s</td>
</tr>
<tr>
<td>Cold Start</td>
<td>&lt; 35</td>
<td>s</td>
</tr>
</tbody>
</table>

TABLE 5 – ACQUISITION TIME

Notes:
1. EVK is 24-hrs. static under signal conditions of -130dBm and ambient temperature of +25°C.
2. Outage duration ≤ 30s.

14.2. SENSITIVITY

14.2.1. TRACKING

Tracking is an ability of receiver to maintain valid satellite ephemeris data.

During tracking receiver may stop output valid position solutions.

Tracking sensitivity defined as minimum GPS signal power required for tracking.
14.2.2. REACQUISITION
Reacquisition follows temporary blocking of GPS signals.
Reacquisition sensitivity defined as minimum GPS signal power required for reacquisition.

14.2.3. NAVIGATION
During navigation receiver consequently outputs valid position solutions.
Navigation sensitivity defined as minimum GPS signal power required for reliable navigation.

14.2.4. HOT START
Hot Start sensitivity defined as minimum GPS signal power required for valid position solution under Hot Start conditions.

14.2.5. AIDED START
Aided Start sensitivity defined as minimum GPS signal power required for valid position solution following aiding process.

14.2.6. COLD START
Cold Start sensitivity defined as minimum GPS signal power required for valid position solution under Cold Start conditions, sometimes referred as ephemeris decode threshold.

<table>
<thead>
<tr>
<th>OPERATION^1</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tracking</td>
<td>-163</td>
<td>dBm</td>
</tr>
<tr>
<td>Reacquisition^2</td>
<td>-162</td>
<td>dBm</td>
</tr>
<tr>
<td>Navigation</td>
<td>-161</td>
<td>dBm</td>
</tr>
<tr>
<td>Hot Start^3</td>
<td>-160</td>
<td>dBm</td>
</tr>
<tr>
<td>Aided Start^4</td>
<td>-156</td>
<td>dBm</td>
</tr>
<tr>
<td>Cold Start</td>
<td>-148</td>
<td>dBm</td>
</tr>
</tbody>
</table>

TABLE 6 – SENSITIVITY

Notes:
1. GPS signal power level approaching antenna, EVK is static and ambient temperature is +25°C.
2. Outage duration ≤ 30s.
3. Hibernate state duration ≤ 5m.
4. Aiding using Broadcast Ephemeris (Ephemeris Push™) or Extended Ephemeris (CGEE™ or SGEE™).

14.3. POWER CONSUMPTION

<table>
<thead>
<tr>
<th>OPERATION^1</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acquisition</td>
<td>72</td>
<td>mW</td>
</tr>
<tr>
<td>Tracking</td>
<td>59</td>
<td>mW</td>
</tr>
<tr>
<td>ATP™ 200:1</td>
<td>9</td>
<td>mW</td>
</tr>
<tr>
<td>PTF™ 30:30m</td>
<td>0.75</td>
<td>mW</td>
</tr>
<tr>
<td>5m Hibernate:10s tracking</td>
<td>1.9</td>
<td>mW</td>
</tr>
<tr>
<td>Hibernate</td>
<td>25</td>
<td>µW</td>
</tr>
</tbody>
</table>

TABLE 7 – POWER CONSUMPTION
14.4. ACCURACY

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FORMAT</th>
<th>MODE</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Position</td>
<td>Horizontal</td>
<td>CEP (50%)</td>
<td>GPS + SBAS</td>
<td>&lt; 2.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>GPS</td>
<td>&lt; 2.5</td>
</tr>
<tr>
<td></td>
<td>Vertical</td>
<td>2dRMS (95%)</td>
<td>GPS + SBAS</td>
<td>&lt; 4.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>GPS</td>
<td>&lt; 5.0</td>
</tr>
<tr>
<td>Velocity</td>
<td>over ground</td>
<td>VEP (50%)</td>
<td>GPS + SBAS</td>
<td>&lt; 3.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>GPS</td>
<td>&lt; 4.0</td>
</tr>
<tr>
<td></td>
<td>Vertical</td>
<td>2dRMS (95%)</td>
<td>GPS + SBAS</td>
<td>&lt; 6.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>GPS</td>
<td>&lt; 7.5</td>
</tr>
</tbody>
</table>

| Velocity² over ground | 50% of samples | < 0.01 | m/s |
| Heading to north | 50% of samples | < 0.01 | ° |
| Time³ | RMS jitter | 1 PPS | ≤ 30 | ns |

TABLE 8 – ACCURACY

14.5. DYNAMIC CONSTRAINS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>Metric</th>
<th>Imperial</th>
</tr>
</thead>
<tbody>
<tr>
<td>Velocity and Altitude⁴</td>
<td>515 m/s and 18,288 m</td>
<td>1,000 knots and 60,000 ft</td>
</tr>
<tr>
<td>Velocity</td>
<td>600 m/s</td>
<td>1,166 knots</td>
</tr>
<tr>
<td>Altitude</td>
<td>-500 m to 24,000 m</td>
<td>-1,640 ft to 78,734 ft</td>
</tr>
<tr>
<td>Acceleration</td>
<td>4 g</td>
<td></td>
</tr>
<tr>
<td>Jerk</td>
<td>5 m/s³</td>
<td></td>
</tr>
</tbody>
</table>

TABLE 9 – DYNAMIC CONSTRAINS

Notes:
1. $V_{CC} = 1.8$ V, module is static under signal conditions of $-130$ dBm, ambient temperature is $+25^\circ$C.
2. EVK is 24-hrs. static, outdoor, ambient temperature is $+25^\circ$C.
3. Speed over ground ≤ 30 m/s.
4. Standard dynamic constrains according to regulatory limitations.

15. POWER MANAGEMENT

15.1. POWER STATES

15.1.1. FULL POWER ACQUISITION
ORG4400 module stays in Full Power Acquisition state until a reliable position solution is made.

15.1.2. FULL POWER TRACKING
Full Power Tracking state is entered after a reliable position solution is achieved. During this state the processing is less intense compared to Full Power Acquisition, therefore power consumption is lower. Full Power Tracking state with navigation update rate at 5 Hz consumes more power compared to default 1 Hz navigation.
15.1.3. CPU ONLY

CPU Only is the transitional state of ATP™ power saving mode when the RF and DSP sections are partially powered off. This state is entered when the satellites measurements have been acquired, but navigation solution still needs to be computed.

15.1.4. STANDBY

Standby is the transitional state of ATP™ power saving mode when RF and DSP sections are completely powered off and baseband clock is stopped.

15.1.5. HIBERNATE

ORG4400 module boots into Hibernate state after power supply applied, drawing only 9μA. When Hibernate state is following Full Power Tracking state current consumption is 14μA. During this state RF, DSP and baseband sections are completely powered off leaving only RTC and Battery-Backed RAM running.
Module will perform Hot Start if stayed in Hibernate state less than 4 hours from last valid position solution.

15.2. BASIC POWER SAVING MODE

Basic power saving mode is elaborating host in straightforward way for controlling transfers between Full Power and Hibernate states.
Current profile of this mode has no hidden cycles of satellite data refresh.
Host may condition transfers by tracking duration, accuracy, satellites in-view or other parameters.

15.3. SELF MANAGED POWER SAVING MODES

Nano Spider module has several self-managed power saving modes tailored for different use cases. These modes provide several levels of power saving with degradation level of position accuracy. Initial operation in Full Power state is a prerequisite for accumulation of satellite data determining location, fine time and calibration of reference clocks.

15.3.1. ADAPTIVE TRICKLE POWER (ATP™)

ATP™ is best suited for applications that require navigation solutions at a fixed rate as well as low power consumption and an ability to track weak signals.
This power saving mode provides the most accurate position among self-managed modes.
In this mode module is intelligently cycled between Full Power state, CPU Only state consuming 14mA and Standby state consuming ≤ 90μA, therefore optimizing current profile for low power operation.
ATP™ period that equals navigation solution update can be 1 second to 10 seconds.
On-time including Full Power Tracking and CPU Only states can be 200ms to 900ms.

FIGURE 3 – ATP™ TIMING
15.3.2. PUSH TO FIX (PTF™)

PTF™ is best suited for applications that require infrequent navigation solutions. In this mode ORG4400 module is mostly in Hibernate state, drawing ≤ 14µA of current, waking up for satellite data refresh in fixed periods of time. PTF™ period can be anywhere between 10 seconds and 2 hours. Host can initiate an instant position report by toggle the ON_OFF pad to wake up the module. During fix trial module will stay in Full Power state until good position solution is estimated or pre-configured timeout for it has expired.

![PTF™ Timing Diagram]

**FIGURE 4 – PTF™ TIMING**

15.3.3. ADVANCED POWER MANAGEMENT (APM™)

APM™ allows power savings while ensuring that the Quality of the Solution (QoS) is maintained when signals level drop.

In APM™ mode the module is intelligently cycled between Full Power and Hibernate states. In addition to setting the position report interval, a QoS specification is available that sets allowable error estimates and selects priorities between position report interval and more power saving.

User may select between Duty Cycle Priority for more power saving and Time Between Fixes (TBF) priority with defined or undefined maximum horizontal error. TBF range is from 10s to 180s between fixes, Power Duty Cycle range is between 5% to 100%. Maximum position error is configurable between 1 to 160m. The number of APM™ fixes is configurable up to 255 or set to continuous.

![APM™ Timing Diagram]

**FIGURE 5 – APM™ TIMING**
16. EXTENDED FEATURES

16.1. ALMANAC BASED POSITIONING (ABP™)
With ABP™ mode enabled, the user can get shorter Cold Start TTFF as tradeoff with position accuracy. When no sufficient ephemeris data is available to calculate an accurate solution, a coarse solution will be provided where the position is calculated based on one or more of the GPS satellites, having their states derived from the almanac data.
Data source for ABP™ may be either stored factory almanac, broadcasted or pushed almanac.

16.2. ACTIVE JAMMER DETECTOR AND REMOVER
Jamming Detector is embedded DSP software block that detects interference signals in GPS L1 band. Jamming Remover is additional DPS software block that sort-out Jamming Detector output mitigating up to 8 interference signals of Continuous Wave (CW) type up to 80dB-Hz each.

16.3. CLIENT GENERATED EXTENDED EPHEMERIS (CGEE™)
CGEE™ feature allows shorter TTFFs by providing predicted (synthetic) ephemeris files created within a non-networked host system from previously received satellite ephemeris data. The prediction process requires good receipt of broadcast ephemeris data for all satellites. EE files created this way are good for up to 3 days and then expire.
CGEE™ feature requires avoidance of power supply removal.
CGEE™ data files are stored and managed by host.

16.4. SERVER GENERATED EXTENDED EPHEMERIS (SGEE™)
SGEE™ enables shorter TTFFs by fetching Extended Ephemeris (EE) file downloaded from web server. Host is initiating periodic network sessions of EE file downloads, storage and provision to module. There is one-time charge for set-up, access to OriginGPS EE distribution server and end-end testing for re-distribution purposes, or there is a per-unit charge for each module within direct SGEE™ deployment.
EE files are provided with look-ahead of 1, 3, 7, 14 or 31 days.
17. INTERFACE

17.1. PAD ASSIGNMENT

<table>
<thead>
<tr>
<th>PAD</th>
<th>NAME</th>
<th>FUNCTION</th>
<th>DIRECTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RESET</td>
<td>Asynchronous Reset</td>
<td>Input</td>
</tr>
<tr>
<td>2</td>
<td>RX</td>
<td>UART Receive</td>
<td>SPI Data In</td>
</tr>
<tr>
<td>3</td>
<td>CTS</td>
<td>Interface Select 1</td>
<td>UART Clear To Send</td>
</tr>
<tr>
<td>4</td>
<td>WAKEUP</td>
<td>Power Status</td>
<td>Output</td>
</tr>
<tr>
<td>5</td>
<td>TX</td>
<td>UART Transmit</td>
<td>SPI Data Out</td>
</tr>
<tr>
<td>6</td>
<td>ON_OFF</td>
<td>Power State Control</td>
<td>Input</td>
</tr>
<tr>
<td>7</td>
<td>1PPS</td>
<td>UTC Time Mark</td>
<td>Output</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>System Ground</td>
<td>Power</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>System Ground</td>
<td>Power</td>
</tr>
<tr>
<td>10</td>
<td>NC</td>
<td>Not Connected</td>
<td>Power</td>
</tr>
<tr>
<td>11</td>
<td>V_CC</td>
<td>System Power</td>
<td>Power</td>
</tr>
<tr>
<td>12</td>
<td>V_CC</td>
<td>System Power</td>
<td>Power</td>
</tr>
<tr>
<td>13</td>
<td>GND</td>
<td>RF Ground</td>
<td>Power</td>
</tr>
<tr>
<td>14</td>
<td>RF_IN</td>
<td>Antenna Signal Input</td>
<td>Analog Input</td>
</tr>
<tr>
<td>15</td>
<td>GND</td>
<td>RF Ground</td>
<td>Power</td>
</tr>
<tr>
<td>16</td>
<td>RTS</td>
<td>Interface Select 2</td>
<td>UART Ready To Send</td>
</tr>
</tbody>
</table>

TABLE 10 – PIN-OUT

Top View

FIGURE 7 -PAD ASSIGNMENT
17.2. POWER SUPPLY

It is recommended to keep the power supply on all the time in order to maintain RTC block active and keep satellite data in RAM for fastest possible TTFF.

When $V_{CC}$ is removed settings are reset to factory default and the receiver performs Cold Start on next power up.

17.2.1. $V_{CC}$

$V_{CC}$ is 1.8V ±5% DC and must be provided from regulated power supply.

Typical $I_{CC}$ is 40mA during acquisition.

Inrush current can be up to 100mA for about 20µs duration, whilst VCC can drop down to 1.7V.

Maximum $I_{CC}$ current in Hibernate state is 15µA, while all I/O lines externally held in Hi-Z state.

Output capacitors are critical when powering module from switch-mode power supply.

Filtering is important to manage high alternating current flows on the power input connection.

An additional LC filter on module power input may be needed to reduce system noise.

The high rate of module input current change requires low ESR bypass capacitors.

Additional higher ESR output capacitors can provide input stability damping.

The ESR and size of the output capacitors directly define the output ripple voltage with a given inductor size. Large low ESR output capacitors are beneficial for low noise.

Voltage ripple below 50mV$_{P-P}$ is allowed for frequencies between 100KHz to 1MHz.

Voltage ripple below 15mV$_{P-P}$ is allowed for frequencies above 1MHz.

Voltage ripple higher than allowed may compromise sensitivity parameter.

17.2.2. GROUND

Ground pads must be connected to host PCB Ground with shortest possible traces or vias.

17.3. RF INPUT

RF input impedance is 50Ω, DC blocked up to 10V.

Nano Spider ORG4400 module supports active or passive antenna.

17.3.1. PASSIVE ANTENNA

In design with passive antenna attention should be paid on antenna layout.

Short trace of 50Ω controlled impedance should conduct GPS signal from antenna to RF_IN pad.

Nano Spider ORG4400 is designed to track GPS signal levels in a range down to close to the thermal noise floor. At low signal levels, control of external noise sources is a significant factor in achieving the best performance of the receiver.

Designing with passive antenna require RF layout skills and can be challenging.

17.3.2. ACTIVE ANTENNA

Active antenna net gain including conduction losses should not exceed +25dB.

DC bias voltage for active antenna can be externally applied on RF_IN trace through bias-T.

DC bias voltage can be controlled by WAKEUP output through MOSFET or load switch.
17.4. CONTROL INTERFACE

17.4.1. ON_OFF

ON_OFF input is used to switch ORG4400 between different power states:

- While in Hibernate state, ON_OFF pulse will initiate transfer into Full Power state.
- While in ATP™ mode, ON_OFF pulse will initiate transfer into Full Power state.
- While in PTF™ mode, ON_OFF pulse will initiate one PTF™ request.
- While in Full Power state, ON_OFF pulse will initiate orderly shutdown into Hibernate state.

![ON_OFF Timing Diagram]

ON_OFF detector set requires a rising edge and high logic level that persists for at least 100µs.
ON_OFF detector reset requires ON_OFF asserted to low logic level for at least 100µs.
Recommended ON_OFF Low-High-Low pulse length is 100ms.
ON_OFF pulses with less than 1s intervals are not recommended.
Multiple switch bounce pulses are recommended to be filtered out.
Pull-down resistor of 10kΩ-33kΩ is recommended to avoid accidental power mode change.
ON_OFF input is tolerable up to 3.6V.
Do not drive high permanently or pull-up this input.
This line must be connected to host.

17.4.2. WAKEUP

WAKEUP output from ORG4400 is used to indicate power state.
A low logic level indicates that the module is in one of its low-power states - Hibernate or Standby. A high logic level indicates that the module is in Full Power state.
Connecting WAKEUP to ON_OFF enables autonomous start to Full Power state.
In addition WAKEUP output can be used to control auxiliary devices.
Wakeup output is LVCMOS 1.8V compatible. Do not connect if not in use.

17.4.3. RESET

Power-on-Reset (POR) sequence is generated internally.
In addition, external reset is available through RESET pad.
Resetting ORG4400 clears the state machine of self-managed power saving modes to default.
RESET signal should be applied for at least 1µs.
RESET input is active low and has internal pull-up resistor of 86kΩ to internal 1.2V domain.
Do not drive this input high. Do not connect if not in use.

17.4.4. 1PPS

Pulse-Per-Second (PPS) output provides a pulse signal for timing purposes.
PPS output starts when position solution has been obtained using 5 or more GPS satellites.
PPS output stops when 3D position solution is lost.
Pulse length (high state) is 200ms with rising edge is less than 30ns synchronized to UTC epoch.
The correspondent UTC time message is generated and put into output FIFO 300ms after the PPS signal. The exact time between PPS and UTC time message delivery depends on message rate, message queue and communication baud rate.
1PPS output is LVCMOS 1.8V compatible. Do not connect if not in use.
17.5. DATA INTERFACE

ORG4400 module has 3 types of interface ports to connect to host - UART, SPI or I2C – all multiplexed on a shared set of pads. At system reset host port interface lines are disabled, so no conflict occurs. Logic values on CTS and RTS are read by the module during startup and define host port type. External resistor of 10kΩ is recommended. Pull-up resistor is referenced to 1.8V.

<table>
<thead>
<tr>
<th>PORT TYPE</th>
<th>CTS</th>
<th>RTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART</td>
<td>External pull-up</td>
<td>Internal pull-up</td>
</tr>
<tr>
<td>SPI (default)</td>
<td>Internal pull-down</td>
<td>Internal pull-up</td>
</tr>
<tr>
<td>I2C</td>
<td>Internal pull-down</td>
<td>External pull-down</td>
</tr>
</tbody>
</table>

**TABLE 11 – HOST INTERFACE SELECT**

17.5.1. UART

UART host interface features are:
- TX used for GPS data reports. Output logic high voltage level is LVCMOS 1.8V compatible.
- RX used for receiver control. Input logic high voltage level is 1.45V, tolerable up to 3.6V.
- UART flow control using CTS and RTS lines is disabled by default. Can be turned on by sending OSP Message ID 178, Sub ID 2 input command.

17.5.2. SPI

SPI host interface features are:
- Slave SPI Mode 1, supports clock up to 6.8MHz.
- RX and TX have independent 2-byte idle patterns of ‘0xA7 0xB4’.
- TX and RX each have independent 1024 byte FIFO buffers.
- TX FIFO is disabled when empty and transmits its idle pattern until re-enabled.
- RX FIFO detects a software specified number of idle pattern repeats and then disables FIFO input until the idle pattern is broken.
- FIFO buffers can generate an interrupt at any fill level.
- SPI detects synchronization errors and can be reset by software.
- Output is LVCMOS 1.8V compatible. Inputs are tolerable up to 3.6V.

17.5.3. I2C

I2C host interface features are:
- I2C Multi-Master Mode - module initiates clock and data, operating speed 400kbps.
- I2C address ‘0x60’ for RX and ‘0x62’ for TX.
- Individual transmit and receive FIFO length of 64 bytes.
- Clock rate can be switched 100KHz (default 400KHz), address can be changed (default 0x62 for TX FIFO and 0x60 for RX FIFO) by sending OSP Message ID 178, Sub ID 2 input command.
- SCL and SDA are pseudo open-drain lines, therefore require external pull-up resistors of 2.2kΩ to 1.8V, or 3.3kΩ to 3.3V.
18. TYPICAL APPLICATION CIRCUIT

18.1. PASSIVE ANTENNA

Designing with passive antenna require RF layout skills and can be challenging. Contact OriginGPS for application specific recommendations and design review services.

18.2. PASSIVE ANTENNA WITH EXTERNAL LNA

![Pictorial Diagram](image)

UART: R1=10K; R2, R5, R6 - DO NOT ASSEMBLE. Use level shifter if MCU_IO level >1.8V

SPI: R1, R2, R5, R6 - DO NOT ASSEMBLE

I2C: R2=10K; R5, R6=2.2K; R1 - DO NOT ASSEMBLE

**FIGURE 9 – SCHEMATIC DIAGRAM OF PASSIVE ANTENNA WITH EXTERNAL LNA**
18.3. ACTIVE ANTENNA

UART: R1=10K; R2, R5, R6 - DO NOT ASSEMBLE. Use level shifter if MCU_IO level >1.0V

SPI: R1, R2, R5, R6 - DO NOT ASSEMBLE

I2C: R2=10K; R5, R6=2.2K; R1 - DO NOT ASSEMBLE

19. RECOMMENDED PCB LAYOUT

19.1. FOOTPRINT

FIGURE 10 – SCHEMATIC DIAGRAM OF ACTIVE ANTENNA CONNECTION

FIGURE 11 – FOOTPRINT

recommended NFA31CC220S1E4 or similar
19.2. RF TRACE

![RF Trace Diagram]

FIGURE 12 – TYPICAL MICROSTRIP PCB TRACE ON FR-4 SUBSTRATE

19.3. PCB STACK-UP

controlled impedance 50Ω

<table>
<thead>
<tr>
<th>CS</th>
<th>Signals</th>
<th>Ground</th>
<th>Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>L₂</td>
<td>Ground</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lₙ</td>
<td>Signals or Power</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>PS</td>
<td>Ground</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

FIGURE 13 – TYPICAL PCB STACK-UP

19.4. PCB LAYOUT RESTRICTIONS

Switching and high-speed components, traces and vias must be kept away from ORG4400 module. Signal traces to/from module should have minimum length. Recommended minimal distance from adjacent active components is 3mm. Ground pads must be connected to host PCB Ground with shortest possible traces or vias. In case of tight integration constrain or co-location with adjacent high speed components like CPU or memory, high frequency components like transmitters, clock resonators or oscillators, LCD panels or CMOS image sensors, contact OriginGPS for application specific recommendations.
20. DESIGN CONSIDERATIONS

ORG4400 operates with received signal levels down to -163dBm and can be affected by high absolute levels of RF signals, moderate levels of RF interference near the GPS bands and by low-levels of RF noise in the GPS band.

RF interference from nearby electronic circuits or radio transmitters can contain enough energy to desensitize ORG4400. These systems may also produce levels of energy outside of GPS band, high enough to leak through RF filters and degrade the operation of the radios in ORG4400.

This issue becomes more critical in small products, where there are industrial design constraints. In that environment, transmitters for Wi-Fi, Bluetooth, RFID, cellular and other radios may have antennas physically close to the GPS antenna.

To prevent degraded performance of ORG4400, OriginGPS recommends performing EMI/jamming susceptibility tests for radiated and conducted noise on prototypes and assessing risks of other factors.

Antennas for GPS and GLONASS have a wider bandwidth than pure GPS antennas. Some wideband antennas may not have a good axial ratio to block reflections of RHCP GPS and GLONASS signals. These antennas have lower rejection of multipath reflections and tend to degrade the overall performance of the receiver.

Designing with passive antenna require RF layout skills and can be challenging. Contact OriginGPS for application specific recommendations and design review services.

21. OPERATION

When power is first applied, ORG4400 goes into a Hibernate state while integrated RTC starts and internal Finite State Machine (FSM) sequences though to “Ready-to-Start” state.

Host is not required to control external master nRESET since module’s internal reset circuitry handles detection of power application.

While in “Ready-to-Start” state, ORG4400 awaits a pulse to the ON_OFF input. Since integrated RTC startup times are variable, host is required either to wait for a fixed interval or to monitor a short Low-High-Low pulse on WAKEUP output that indicates FSM “Ready-to-Start” state.

Another option is to repeat a pulse on the ON_OFF input every second until the module starts by either detecting a stable logic high level on WAKEUP output or by generation of UART messages.

21.1. STARTING THE MODULE

A pulse on the ON_OFF input line when FSM is ready and in startup-ready state, Hibernate state, standby state, will command the module to start.

ON_OFF detector set requires a rising edge and high logic level that persists for at least 100µs.

ON_OFF detector reset requires ON_OFF asserted to low logic level for at least 100µs.

Recommended ON_OFF Low-High-Low pulse length is 100ms.

ON_OFF pulses with less than 1s intervals are not recommended.
21.2. AUTONOMOUS POWER ON
Connecting WAKEUP output (pad 4) to ON_OFF input (pad 6) enables self-start to Full Power state from Ready-To-Start state following boot process.
When host data interface is set UART, module will start autonomously transmitting NMEA messages after first power supply application. Further transfers between Full Power and Hibernate states require external logic circuitry combined with serial command.

21.3. VERIFYING THE MODULE HAS STARTED
WAKEUP output will go high indicating ORG4400 has started.
System activity indication depends upon selected serial interface. The first message to come out of module is “OK_TO_SEND” - ‘$PSRF150,1*3E’.
21.3.1. UART
When active, the module will output NMEA messages at 4800bps.

21.3.2. I²C
In Multi-Master mode with no bus contention - the module will spontaneously send messages.
In Multi-Master mode with bus contention - the module will send messages after the I²C bus contention resolution process allows it to send.

21.3.3. SPI
Since ORG4400 is SPI slave device, there is no possible indication of system “ready” through SPI interface. Host must initiate SPI connection approximately 1s after WAKEUP output goes high.

21.4. SHUTTING DOWN THE MODULE
Transferring module from Full Power state to Hibernate state can be initiated in two ways:

+ By a pulse on ON_OFF input.
+ By NMEA ($PSRF117) or OSP (MID205) serial message.

Orderly shutdown process may take anywhere from 10ms to 900ms to complete, depending upon operation in progress and messages pending, and hence is dependent upon serial interface speed and controls. Module will stay in Full Power state until TX FIFO buffer is emptied.
The last message during shutdown sequence is ‘$PSRF150,0*3F’.
22. FIRMWARE

22.1. DEFAULT SETTINGS

<table>
<thead>
<tr>
<th>Setting</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power On State</td>
<td>Hibernate</td>
</tr>
<tr>
<td>Default Interface(^1)</td>
<td>SPI</td>
</tr>
<tr>
<td>SPI Data Format</td>
<td>NMEA</td>
</tr>
<tr>
<td>UART Settings</td>
<td>4,800bps</td>
</tr>
<tr>
<td>UART Data Format</td>
<td>NMEA</td>
</tr>
<tr>
<td>I²C Settings</td>
<td>Multi-Master 400kbps</td>
</tr>
<tr>
<td>I²C Data Format</td>
<td>NMEA</td>
</tr>
<tr>
<td>Satellite Constellation</td>
<td>GPS</td>
</tr>
<tr>
<td>Default Output Messages</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$GPGGA @1 sec.</td>
</tr>
<tr>
<td></td>
<td>$GPGSA @ 1 sec.</td>
</tr>
<tr>
<td></td>
<td>$GPGSV @ 5 sec.</td>
</tr>
<tr>
<td></td>
<td>$GPRMC @ 1 sec.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Firmware Defaults</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SBAS</td>
<td>OFF</td>
</tr>
<tr>
<td>ABP(^\text{TM})</td>
<td>OFF</td>
</tr>
<tr>
<td>Static Navigation</td>
<td>OFF</td>
</tr>
<tr>
<td>Track Smoothing</td>
<td>OFF</td>
</tr>
<tr>
<td>Jammer Detector</td>
<td>ON</td>
</tr>
<tr>
<td>Jammer Remover</td>
<td>OFF</td>
</tr>
<tr>
<td>Fast Time Sync</td>
<td>OFF</td>
</tr>
<tr>
<td>Pseudo DR Mode</td>
<td>ON</td>
</tr>
<tr>
<td>Power Saving Mode</td>
<td>OFF</td>
</tr>
<tr>
<td>3SV Solution Mode</td>
<td>ON</td>
</tr>
<tr>
<td>5Hz Update Rate</td>
<td>OFF</td>
</tr>
</tbody>
</table>

TABLE 13 – DEFAULT FIRMWARE SETTINGS

Note:
1. Without external resistor straps on CTS or RTS.

22.2. FIRMWARE UPDATES

Firmware updates can be considered exclusively as patches on top of baseline ROM firmware. Those patch updates may be provided from time to time to address ROM firmware issues as a method of performance improvement. Typical patch file size is 24KB.

Host controller is initiating load and application of patch update by communicating module’s Patch Manager software block allocating 16KB of memory space for patch and additional 8KB for cache. Patch updates are preserved until BBRAM is discarded.
23. HANDLING INFORMATION

23.1. MOISTURE SENSITIVITY

ORG4400 modules are MSL 3 designated devices according to IPC/JEDEC J-STD-033B standard. Module in sample or bulk package should be baked prior to assembly at 125°C for 48 hours.

23.2. ASSEMBLY

The module supports automatic pick-and-place assembly and reflow soldering processes. Please refer to the following recommendations for Stencil and Solder Paste:

- Stencil thickness of fewer than 4 mils.
- Stencil radius opening ratio 80%-110% of a pad.
- Stencil type EFAB or Laser cut fine-grained material for high solder paste release.
- Solder paste type 4.5 up to type 6 target small size ball paste.

23.3. SOLDERING

Reflow soldering of the module always on component side (Top side) of the host PCB according to standard IPC/JEDEC J-STD-020D for LGA SMD. Avoid exposure of ORG4400 to face-down reflow soldering process.

![Recommended Soldering Profile Diagram](image)

FIGURE 16 – RECOMMENDED SOLDERING PROFILE

Referred temperature is measured on top surface of the package during the entire soldering process. Suggested peak reflow temperature is 245°C for 30 sec. for Pb-Free solder paste. Actual board assembly reflow profile must be developed individually per furnace characteristics. Reflow furnace settings depend on the number of heating/cooling zones, type of solder paste/flux used, board design, component density and packages used.
23.4. CLEANING

If flux cleaning is required, module is capable to withstand standard cleaning process in vapor degreaser with the Solvon® n-Propyl Bromide (NPB) solvent and/or washing in DI water. Avoid cleaning process in ultrasonic degreaser, since specific vibrations may cause performance degradation or destruction of internal circuitry.

23.5. REWORK

If localized heating is required to rework or repair the module, precautionary methods are required to avoid exposure to solder reflow temperatures that can result in permanent damage to the device.

23.6. ESD SENSITIVITY

This product is ESD sensitive device and must be handled with care.

23.7. SAFETY INFORMATION

Improper handling and use can cause permanent damage to the product.

23.8. DISPOSAL INFORMATION

This product must not be treated as household waste.

For more detailed information about recycling electronic components contact your local waste management authority.

---

**TABLE 14 – SOLDERING PROFILE PARAMETERS**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_c$</td>
<td>Classification Temp.</td>
<td>245</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$T_p$</td>
<td>Package Temp.</td>
<td></td>
<td>245</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$T_l$</td>
<td>Liquidous Temp.</td>
<td>217</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$T_s$</td>
<td>Soak/Preheat Temp.</td>
<td>150</td>
<td>200</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$t_s$</td>
<td>Soak/Preheat Time</td>
<td>60</td>
<td>120</td>
<td></td>
<td>s</td>
</tr>
<tr>
<td>$t_l$</td>
<td>Liquidous Time</td>
<td>60</td>
<td>150</td>
<td></td>
<td>s</td>
</tr>
<tr>
<td>$t_p$</td>
<td>Peak Time</td>
<td></td>
<td>30</td>
<td></td>
<td>s</td>
</tr>
</tbody>
</table>
24. MECHANICAL SPECIFICATIONS

- ORG4400 module has advanced ultra-miniature LGA SMD packaging sized 4.1mm x 4.1mm.
- On bottom side there are 16 LGA SMT pads with Cu base and ENIG plating.
- ORG4400 module supports automated pick and place assembly and reflow soldering processes.

![TOP VIEW](image1)
![SIDE VIEW](image2)
![BOTTOM VIEW](image3)

FIGURE 17 – MECHANICAL DRAWING

<table>
<thead>
<tr>
<th>Dimensions</th>
<th>Length</th>
<th>Width</th>
<th>Height</th>
<th>Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>4.10 ±0.10/-0.05</td>
<td>4.10±0.10/-0.05</td>
<td>2.1 ±0.1/-0.0</td>
<td>gr</td>
</tr>
<tr>
<td>inch</td>
<td>0.161 ±0.004/-0.002</td>
<td>0.161±0.004/-0.002</td>
<td>0.083 ±0.004/-0.0</td>
<td>oz</td>
</tr>
</tbody>
</table>

TABLE 15 – MECHANICAL SUMMARY

25. COMPLIANCE

The following standards are applied on the production of ORG4400 modules:

- IPC-6011/6012 Class2 for PCB manufacturing
- IPC-A-600 Class2 for PCB inspection
- IPC-A-610D Class2 for SMT acceptability

ORG4400 modules are manufactured in ISO 9001:2008 accredited facilities.
ORG4400 modules are manufactured in ISO 14001:2004 accredited facilities.
ORG4400 modules are manufactured in OHSAS 18001:2007 accredited facilities.
ORG4400 modules are designed, manufactured and handled in compliance with the Directive 2011/65/EU of the European Parliament and of the Council of June 2011 on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment, referred as RoHS II.
ORG4400 modules are manufactured and handled in compliance with the applicable substance bans as of Annex XVII of Regulation 1907/2006/EC on Registration, Evaluation, Authorization and Restriction of Chemicals including all amendments and candidate list issued by ECHA, referred as REACH.
ORG4400 modules comply with the following EMC standards:

- EU CE EN55022:06+A1(07), Class B
- JAPAN VCCI V-3/2006.04
26. PACKAGING AND DELIVERY

26.1. APPEARANCE

ORG4400 modules are delivered in reeled tapes for automatic pick and place assembly process.

![Reel Diagram]

FIGURE 18 – MODULE POSITION

ORG4400 modules are packed in 2 different reel types.

<table>
<thead>
<tr>
<th>SUFFIX</th>
<th>TR1</th>
<th>TR2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantity</td>
<td>500</td>
<td>2000</td>
</tr>
</tbody>
</table>

TABLE 16 – REEL QUANTITY

Reels are dry packed with humidity indicator card and desiccant bag according to IPC/JEDEC J-STD-033B standard for MSL 3 devices.
Reels are vacuum sealed inside anti-static moisture barrier bags.
Sealed reels are labeled with MSD sticker providing information about:
+ MSL
+ Shelf life
+ Reflow soldering peak temperature
+ Seal date

Sealed reels are packed inside cartons.
Reels, reel packs and cartons are labeled with sticker providing information about:
+ Description
+ Part number
+ Lot number
+ Customer PO number
+ Quantity
+ Date code
26.2. CARRIER TAPE
Carrier tape material - polystyrene with carbon (PS+C).
Cover tape material – polyester based film with heat activated adhesive coating layer.

![Figure 19 - Carrier Tape]

<table>
<thead>
<tr>
<th>mm</th>
<th>inch</th>
</tr>
</thead>
<tbody>
<tr>
<td>A₀</td>
<td>4.35 ± 0.1</td>
</tr>
<tr>
<td>B₀</td>
<td>4.35 ± 0.1</td>
</tr>
<tr>
<td>K₀</td>
<td>2.30 ± 0.1</td>
</tr>
<tr>
<td>W</td>
<td>12.0 ± 0.3</td>
</tr>
</tbody>
</table>

26.3. REEL
Reel material - antistatic plastic.

![Figure 20 - Reel]

<table>
<thead>
<tr>
<th>SUFFIX</th>
<th>TR1</th>
<th>TR2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Mm</td>
<td>Inch</td>
</tr>
<tr>
<td>ØA</td>
<td>178.0 ± 1.0</td>
<td>7.00 ± 0.04</td>
</tr>
<tr>
<td>ØN</td>
<td>60.0 ± 1.0</td>
<td>2.36 ± 0.04</td>
</tr>
<tr>
<td>W₁</td>
<td>12.7 ± 0.5</td>
<td>0.50 ± 0.02</td>
</tr>
<tr>
<td>W₂</td>
<td>15.8 ± 0.5</td>
<td>0.62 ± 0.02</td>
</tr>
</tbody>
</table>
27. ORDERING INFORMATION

![Ordering Options Diagram]

**TABLE 19 – ORDERING OPTIONS**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>FIRMWARE VERSION</th>
<th>HARDWARE VARIANT</th>
<th>PACKAGING</th>
<th>SPQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>ORG4400-PM04-TR1</td>
<td>3</td>
<td>01</td>
<td>REELED TAPE</td>
<td>500</td>
</tr>
<tr>
<td>ORG4400-PM04-TR2</td>
<td>3</td>
<td>01</td>
<td>REELED TAPE</td>
<td>2000</td>
</tr>
<tr>
<td>ORG4400-PM04-UAR</td>
<td>3</td>
<td>01</td>
<td>EVALUATION KIT</td>
<td>1</td>
</tr>
</tbody>
</table>

**TABLE 20 – ORDERABLE DEVICES**
28. I2C Appendix

I2C host interface features are:

- I2C Multi-Master mode - module initiates clock and data, default operating speed 400kbps.
- I2C address ‘0x60’ for commands from controller to GPS-module. (Default)
- I2C address ‘0x62’ for the data transmits from the GPS-module to the host. (Default)
- Individual transmit and receive FIFO length of 64 bytes.
- SCL and SDA are pseudo open-drain lines, therefore require external pull-up resistors of 2.2kΩ to 1.8V, or 3.3kΩ to 3.3V.
- Multi-Master mode – the Host (MCU) can operate either in Slave mode or Multi-Master mode (more common). If MCU is acting as slave, then it can only listen to the GPS. If you want to send any configuration commands to GPS, then host needs to be in Master or Multi master mode.
- While Host (MCU) is in Master/Multi-Master mode, the following can be changed:
  1) Clock rate can be switched to 100KHz (OSP command).
  2) I2C address, (OSP command)
  3) OSP/NMEA mode
  4) GPS can be turn into a Slave mode by sending OSP Message ID 178, Sub ID 2 input command.

Change the GPS module from Multi master to Slave mode:
  a. change from NMEA to OSP - “$PSRF100,0,115200,8,1,0*04\n”.
  b. Change to Slave mode with 400Kbps, send:
  c. A0 A2 00 39 B2 02 00 F9 C5 68 03 FF 00 00 0B B8 09 0B 38 F9 00 01 03 FC 03 FC 00 04 00 3E 00 00 00 7C 00 00 00 00 00 00 00 00 00 00 00 00 00 00 01 C2 00 00 00 62 00 60 01 00 01 F4 00 01 0B 1D B0 B3 0D 0A
  d. Read 128 Bytes at least from the GPS module, and then immediately without any delay send the next OSP message.
  e. If you want to switch back from OSP to NMEA please use command
     A0 A2 00 18 81 00 01 01 01 01 01 01 05 01 01 01 01 01 01 01 01 00 00 01 01 00 12 C0 01 66 B0 B3

<table>
<thead>
<tr>
<th>GPS multi master</th>
<th>Host Slave</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C address ‘0x60’</td>
<td>I2C address ‘0x62’</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GPS slave</th>
<th>Host Master</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C address ‘0x60’</td>
<td>I2C any address</td>
</tr>
</tbody>
</table>