SPIDER
ORG4472
GPS RECEIVER MODULE

DATASHEET

1. Introduction

ORG4472 module is industry's smallest, autonomous, fully featured GPS engine.

ORG4472 module is miniature multi-channel receiver that continuously tracks all satellites in view and provides accurate positioning data in industry's standard NMEA format.

Internal ARM CPU core and sophisticated firmware keep GPS payload off the host and allow integration in low resources embedded solutions.

Featuring OriginGPS proprietary Noise-Free Zone System (NFZ™) technology ORG4472 offers the ultimate in high sensitivity GPS performance in small size.
ORG4472 module is complete SiP (System-in-Package) featuring advanced miniature packaging technology and an ultra small footprint designed to commit unique integration features for high volume, low power and cost sensitive applications.

ORG4472 module incorporates SiRFstarIV™ GPS processor.

The revolutionary SiRFstarIV™ architecture is optimized for how people really use location-aware products: often indoors with periods of unobstructed sky view when moving from place to place.

This new architecture can detect changes in context, temperature, and satellite signals to achieve a state of near continuous availability by maintaining and opportunistically updating its internal fine time, frequency, and satellite Ephemeris data while consuming mere microwatts of battery power.

2. Description

OriginGPS has researched and enhanced the performance of standard GPS receivers in real-life applications.
Case study of the specifications of key components through involvement in R&D effort of major vendors derived in highest performance in industry's smallest footprint parts available.
These carefully selected key components resulted in higher sensitivity, faster position fix, navigation stability and operation robustness under rapid environmental changes creating hard-to-achieve laboratory performance in heavy-duty environment.

2.1. Features

- Stand alone operation
- OriginGPS Noise Free Zone System (NFZ™) technology
- Integrated LNA, SAW Filter, TCXO and RTC
- SiRFstarIV™ GSD4e GPS processor
- L1 frequency, C/A code
- 48 track verification channels
- Navigation sensitivity: -160dBm
- Tracking sensitivitv: -163dBm for indoor fixes
- Fast TTFF: < 35s under Cold Start conditions
  < 1s under Hot Start conditions
- Multipath mitigation and indoor tracking
- Active Jammer Remover: tracks up to 8 CW interferers and removes jammers up to 80dB-Hz
- SBAS (WAAS, EGNOS, MSAS) support
- Almanac Based Positioning (ABP™)
- Client Generated Extended Ephemeris (CGEE™) and Server Generated Extended Ephemeris (SGEE™) for very fast TTFFs are supported through SiRFInstantFix™ and SiRFInstantFixII™
- Assisted GPS (A-GPS) support
- Automatic and user programmable power saving scenarios: ATP™, PTF™, APM™
- Low power consumption: <10mW during ATP™
- ARM7® 109MHz baseband CPU
- Smart sensor I^2C master interface
- Selectable UART, SPI or I^2C host interface
- Programmable communication protocol and message rate
- Selectable NMEA or OSP (SiRF Binary) communication standards
- Single voltage supply: 1.8V
- DC blocked 50Ω antenna input
- Ultra small footprint: 7mm x 7mm
- Surface Mount Device (SMD)
- Optimized for automatic assembly and reflow equipment
- Industrial operating temperature range: -40^0 to 85^0C
- Pb-Free RoHS compliant

2.2. Architecture

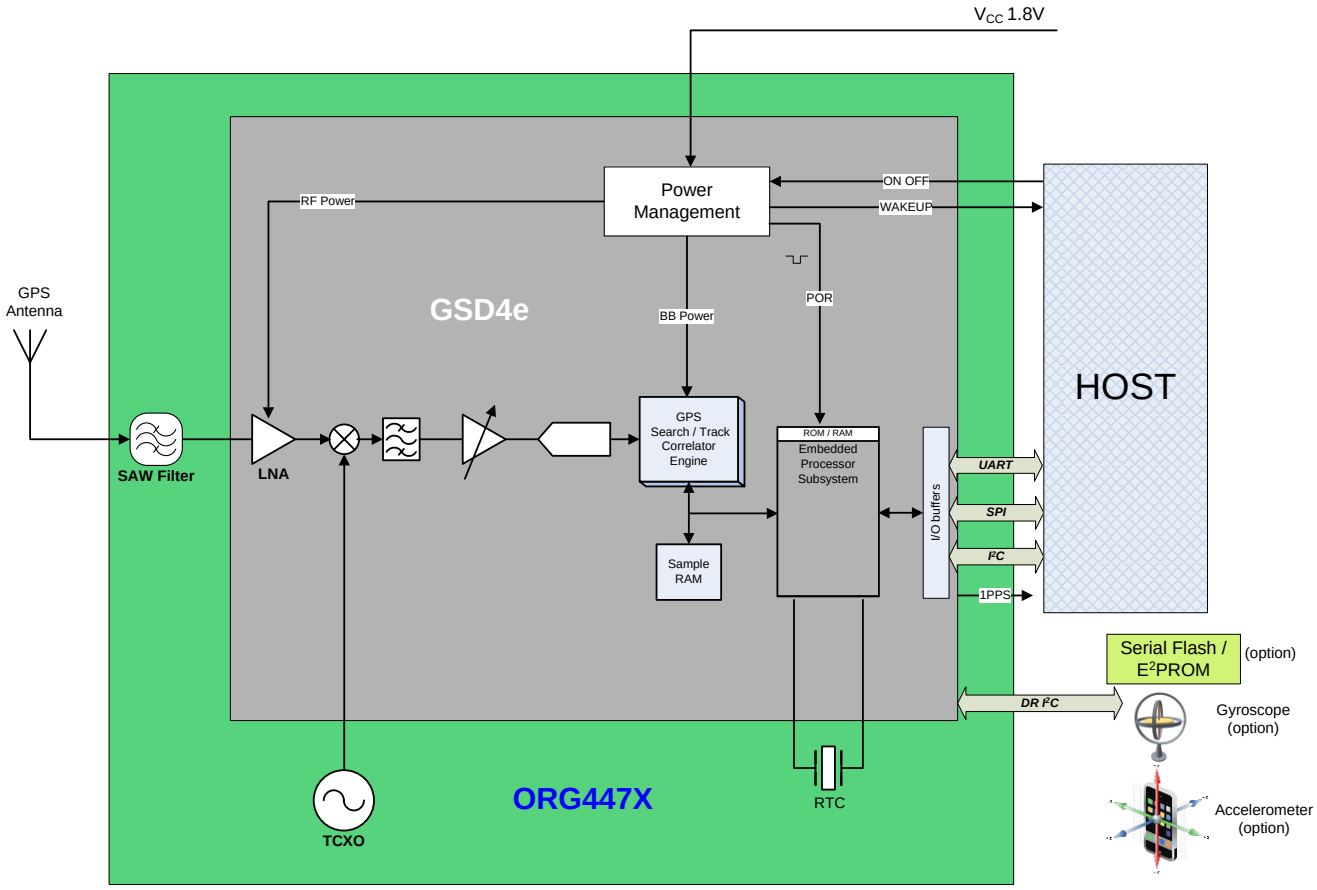


Figure 2-1: ORG4472 architecture

- **Band-pass SAW filter**
  Band-pass SAW filter eliminates inter-modulated out-of-band signals that may corrupt GPS receiver performance.

- **LNA (Low Noise Amplifier)**
  The integrated LNA amplifies the GPS signal to meet RF down converter input threshold. Noise figure optimized design was implemented to provide maximum sensitivity.

- **TCXO (Temperature Compensated Crystal Oscillator)**
  This highly stable 16.369 MHz oscillator controls the down conversion process in RF block. Highest characteristics of this component are key factors in fast TTFF.

- **RTC (Real Time Clock) crystal**
  This miniature component with very tight specifications is necessary for maintaining Hot start and Warm start capabilities.

- **RF shield**
  RF enclosure avoids external interference to compromise sensitive circuitry inside the receiver.
  RF shield is also blocks module's internal emissions from being transmitted.

- **GSD4e IC**

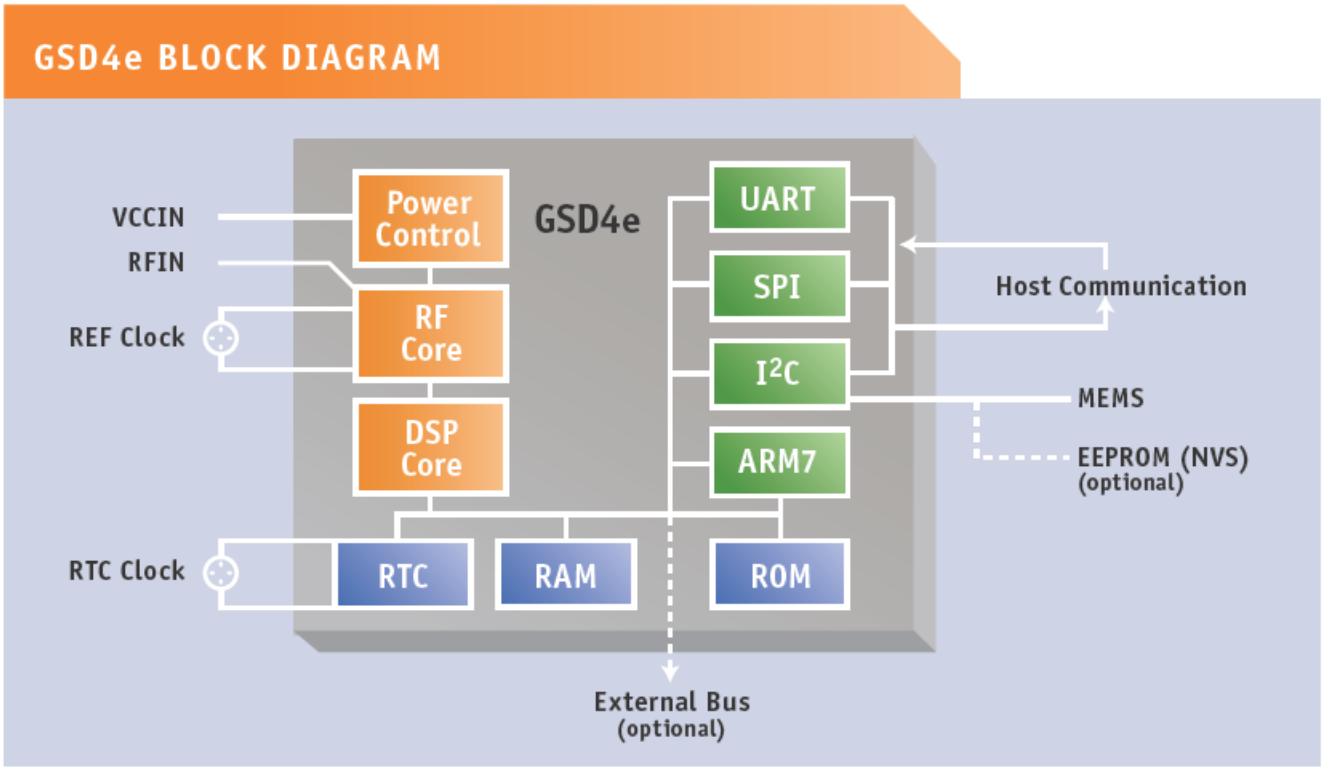


Figure 2-2: GSD4e functional block diagram

SiRFstarIV™ GSD4e GPS processor includes the following units:

- GPS RF core incorporating LNA, down converter, fractional-N synthesizer and ADC block with selectable 2 and 4-bit quantization
- GPS DSP core incorporating more than twice the clock speed and more than double the RAM capacity relative to predecessor - market benchmarking SiRFStarIII™ DSP core
- ARM7® microprocessor system incorporating 109MHz CPU and interrupt controller
- ROM block as code storage for PVT applications
- RAM block for data cache
- RTC block
- UART block
- SPI block
- I^2C block
- Power control block for internal voltage domains management

2.3. Applications

ORG4472 GPS receiver modules have been designed to address new markets where ultra small size and high performance does commit to traditional GPS modules demand for standalone operation, high level of integration, power consumption and design flexibility. ORG4472 module is ideal for standard positioning and navigation applications including indoor tracking:

- Personal locators
- Pet collars
- People and animal tracking systems
- Asset tracking SKU systems
- Sports and recreation accessories
- Handheld consumer navigation and multifunction devices
- Rescue and emergency systems
- Precise timing devices
- Micro robots and micro UAVs
- Automatic Vehicle Location
- Automotive navigation
- Workforce management
- Railway monitoring
- GIS and mapping
- Civil engineering
- Agriculture automation
- Maritime navigation
- Electronic Toll Collection
- Automotive security systems
- Data loggers
- Weather balloons
- WiMAX base stations, Femto and Pico cells
- Industrial sensor platforms
- Location Based Services
- Scientific applications

3. Electrical Specifications

3.1. Absolute Maximum Ratings

Absolute Maximum Ratings are stress ratings only.

Stresses exceeding Absolute Maximum Ratings may damage the device.

Parameter		Symbol	Min	Max	Units
Power Supply Voltage		V_{CC}	-	2.2	V
RF Input Voltage		V_{RF_IN}	-50	50	V
Power Dissipation		P_D	-	200	mW
I/O Voltage		V_{IO}	-0.3	3.6	V
I/O Source/Sink Current		I_{IO}	-10	+10	mA
RF Input Power	f_{IN} = 1560MHz÷1590MHz	P_{RF_IN}	-	10	dBm
	f_{IN} <1560MHz, >1590MHz		-	+15	dBm
ESD Rating	I/O pads	$V_{IO(ESD)}$	-2	+2	kV
	RF input pad	$V_{RF(ESD)}$	-1	+1	kV
Storage temperature		T_{ST}	-55	+125	^{0}C
Lead temperature (10 sec. @ 1mm from case)		T_{LEAD}	-	+260	^{0}C

Table 3-1: Absolute maximum ratings

3.2. Recommended Operating Conditions

Functional operation above the Recommended Operating Conditions is not implied.

Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Parameter	Symbol	Mode / Pad	Test Conditions	Min	Typ	Max	Units
Power supply voltage	V_{CC}			1.71	1.80	1.89	V
Power Supply Current	I_{CC}	Acquisition	-130dBm (Outdoor) $T_{AMB} = 25^0C$		37	47	mA
		Tracking		5		37	mA
		CPU only[1]			14		mA
		Standby[1]			90		µA
		Hibernate			20	25	µA
Input Voltage Low State	V_{IL}	GPIO				0.45	V
Input Voltage High State	V_{IH}			$0.70 \cdot V_{CC}$		3.6	V
Output Voltage Low State	V_{OL}		I_{OL} = 2mA			0.40	V
Output Voltage High State	V_{OH}		I_{OH} = -4mA	$0.75 \cdot V_{CC}$	V_{CC}-0.1		V
Input Capacitance	C_{IN}				4	10	pF
Internal Pull-up Resistor	R_{PU}			50	86	157	kΩ
Internal Pull-down Resistor	R_{PD}			51	91	180	kΩ
Input Leakage Current	$I_{IN(leak)}$		V_{IN} = 1.8V or 0V	-10		+10	µA
Output Leakage Current	$I_{OUT(leak)}$		V_{OUT} = 1.8V or 0V	-10		+10	µA
Input Impedance	Z_{IN}	RF Input	f_0 = 1575.5 MHz		50		Ω
Input Return Loss	RL_{IN}				-8		dB
Operating Temperature[2]	T_{AMB}			-40	+25	+85	^0C
Relative Humidity	RH		Oper. Temp.	5		95	%

Table 3-2: Operating conditions

Notes:
1. Transitional states of ATP™ low power mode
2. Operation below -30^0C to -40^0C is accepted, but TTFF may increase

4. Performance

4.1. Acquisition Times

TTFF (Time To First Fix) – is the period of time from GPS power-up till position estimation.

Hot Start
A hot start results from software reset after a period of continuous navigation or a return from a short idle period that was preceded by a period of continuous navigation. In this state, all of the critical data (position, velocity, time, and satellite ephemeris) is valid to the specified accuracy and available in SRAM.

Warm Start
A warm start typically results from user-supplied position and time initialization data or continuous RTC operation with an accurate last known position available in memory. In this state, position and time data are present and valid, but ephemeris data validity has expired.

Cold Start
A cold start acquisition results when either position or time data is unknown. Almanac information is used to identify previously healthy satellites.

Aided Start
Aiding is a method of effectively reducing the TTFF by making every start Hot or Warm.

	TTFF	Test Condition	Signal Level
Hot Start	< 1s	Outdoor	-130 dBm
Aided Start[1]	< 10s	Outdoor	-130 dBm
Warm Start	< 32s	Outdoor	-130 dBm
Cold Start	< 35s	Outdoor	-130 dBm
Signal Reacquisition	< 1s	Outdoor	-130 dBm

Table 4-1: Acquisition times (typical)

4.2. Sensitivity

	Signal Level
Tracking	-163 dBm
Navigation	-161 dBm
Aided[1]	-156 dBm
Cold Start	-148 dBm

Table 4-2: Sensitivity

Note:
1.Host-assisted device by SGEE™ or self-assisted by CGEE™ or Ephemeris push

4.3. Power Consumption

Operation Mode	Power
Acquisition	67mW
Tracking	9 - 67mW
Hibernate	36µW

Table 4-4: Power consumption (typical)

4.4. Accuracy

		Method	Accurac	Units	Test Conditions	Signal Level
Position	Horizontal	CEP (50%)	< 2.5	m	Outdoor, 24-hr. static	-130 dBm
			< 2	m	Outdoor, 24-hr. static , SBAS on	-130 dBm
		2dRMS (95%)	< 5	m	Outdoor, 24-hr. static	-130 dBm
			< 4	m	Outdoor, 24-hr. static , SBAS on	-130 dBm
	Vertical	VEP (50%)	< 4	m	Outdoor, 24-hr. static	-130 dBm
			< 3	m	Outdoor, 24-hr. static , SBAS on	-130 dBm
		2dRMS (95%)	< 7.5	m	Outdoor, 24-hr. static	-130 dBm
			< 6	m	Outdoor, 24-hr. static , SBAS on	-130 dBm
Velocity	Horizontal	50%	< 0.01	m/s	Outdoor, 30 m/s	-130 dBm
Heading		50%	< 0.01	0	Outdoor, 30 m/s	-130 dBm
Time		1 PPS	< 1	µs	Outdoor	-130 dBm

Table 4-5: Accuracy

4.5. Dynamic Constrains[1]

Velocity <	515 m/s	1,000 knots
Acceleration <	4g	
Altitude <	18,288 m	60,000 ft.

Table 4-6: Dynamic constrains

Note:
1. Standard dynamic constrains according to regulatory limitations

5. Power Management

5.1. Power states

Full Power state (Acquisition/Tracking)
The module stays in full power until a position solution is made and estimated to be reliable. During the acquisition, processing is more intense than during tracking, thus consuming more power.

CPU Only state
This is the state when the RF and DSP sections are partially powered off.
The state is entered when the satellites measurements have been acquired but the navigation solution still needs to be computed.

Standby state
This is the state when the RF and DSP sections are completely powered off and baseband clock is stopped.

Hibernate state
In this state the RF, DSP and baseband sections are completely powered off leaving only the RTC and Battery-Backed RAM running.
The module will perform Hot Start if held in Hibernate state less than 2 hours after valid position solution was acquired.

5.2. Power saving modes

ORG4472 module has three power management modes – ATP™, APM™ and PTF™. These modes provide different levels of power saving with different degradation level of position accuracy.

Adaptive Trickle Power (ATP™)

Adaptive Trickle Power (ATP™) is best suited for applications that require navigation solutions at a fixed rate as well as low power consumption and an ability to track weak signals.
This power saving mode provides the most accurate positioning.
In ATP™ mode ORG4472 module is intelligently cycled between Full Power, CPU Only and Standby states to optimize low power operation.

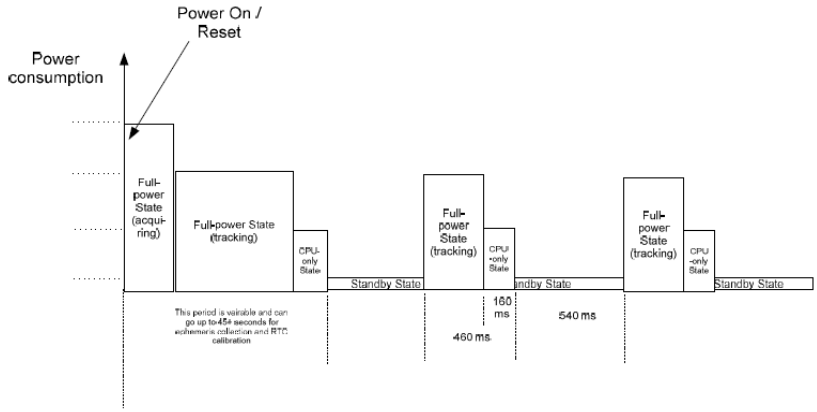


Figure 5-1: ATP™ timing

Push-To-Fix (PTF™)

Push-To-Fix (PTF™) is best suited for applications that require infrequent navigation solutions, optimizing battery life time.
In PTF™ mode ORG4472 module is mostly in Hibernate state, waked up for Ephemeris and Almanac refresh in fixed periods of time.
The PTF™ period is 30 minutes by default but can be anywhere between 10 seconds and 2 hours. When the PTF™ mode is enabled the receiver will stay in Full Power state until the good navigation solution is computed.
When the application needs a position report it can toggle the ON_OFF pad to wake up the module. In this case, a new PTF™ cycle with default settings begins.

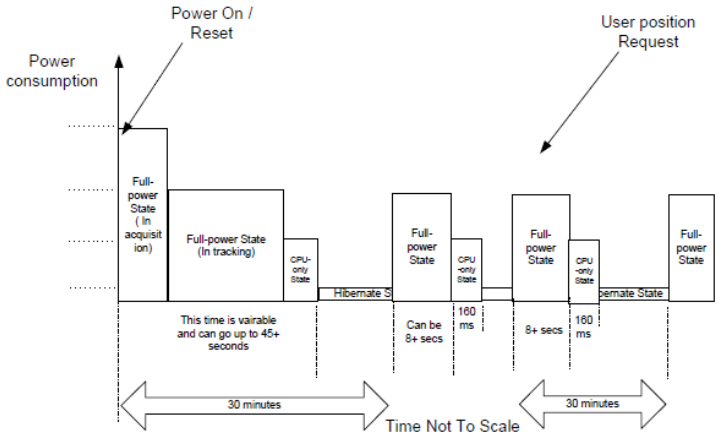


Figure 5-2: PTF™ timing

Advanced Power Management (APM™)

Advanced Power Management (APM™) is designed to give the user more options to configure the power management. The APM™ mode allows power savings while ensuring that the Quality of the Solution (QoS) in maintained when signals level drop.
In addition to setting the position report interval, a QoS specification is available that sets allowable error estimates and selects priorities between position report interval and more power saving. The user may select between Duty Cycle Priority for more power saving and TBF (Time Between Fixes) Priority with defined or undefined maximum horizontal error. TBF range is from 10 to 180 sec. between fixes, Power Duty Cycle range is between 5 to 100%. Maximum position error is configurable between 1 to 160m.
The number of APM™ fixes is configurable up to 255 or set to continuous.
In APM™ mode the module is intelligently cycled between Full Power and Hibernate states.

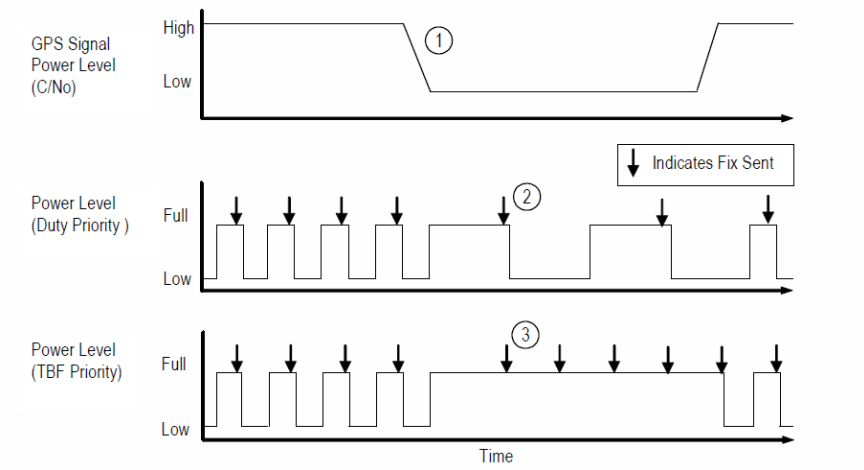


Figure 5-2: APM™ timing

1. GPS signal level drops (e.g user walks indoors)
2. Lower signal results in longer ON time. To maintain Duty Cucle, OFF time is increased.
3. Lower signal means missed fix. To maintain future TBFs, the module goes info Full Power state until signal levels improve.

6. Extended Features

6.1. Almanac Based Positioning (ABP™)

With ABP™ mode enabled, the user can get shorter Cold Start TTFF as a tradeoff with the position error.
When no sufficient Ephemeris data is available to calculate an accurate solution, a coarse solution will be provided where the position is calculated based on one or more of the SVs having their states derived from Almanac data.
Almanac data for ABP™ purposes may be stored factory set, broadcasted or pushed.

6.2. Active Jammer Remover

Jamming Remover is an embedded DSP block that detects, tracks and removes up to 8 Continuous Wave (CW) type signals of up to 80dB-Hz each. Jamming Remover is effective only against continuous narrow band interference signals and covers GPS L1 frequency ±4MHz.

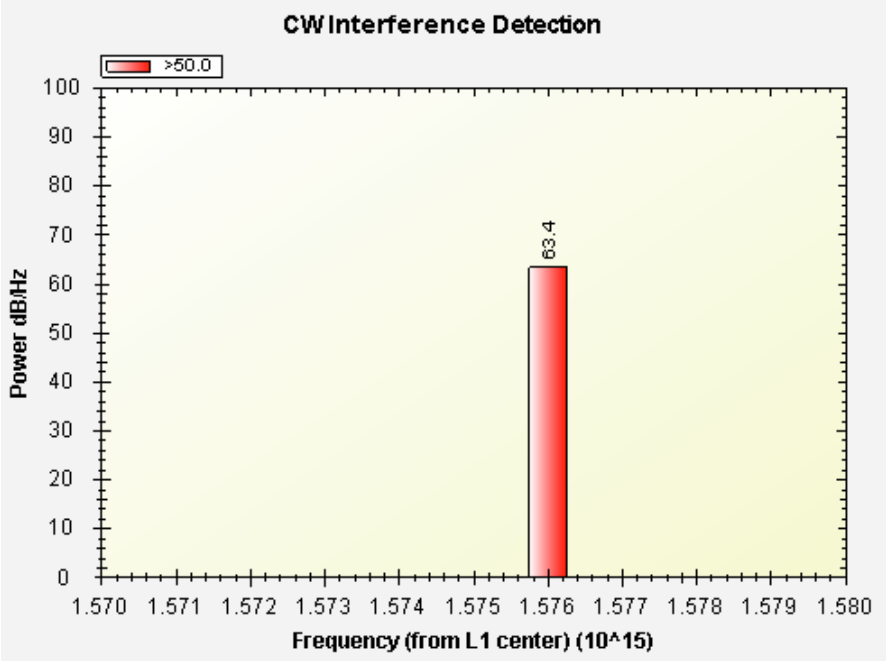


Figure 6-1: Active Jammer Detection frequency plot

6.3. Client Generated Extended Ephemeris (CGEE™)

The CGEE™ feature allows shorter TTFF by providing predicted (synthetic) ephemeris files created within a lost host system from previously received broadcast Ephemeris.
The prediction process requires good receipt of broadcast Ephemeris data for all satellites.
EE files created this way are good for up to 3 days and then expire.
The CGEE™ feature requires avoidance of power supply removal.
CGEE™ data files are stored on internal or external EEPROM or Serial Flash and managed by the receiver or storage and management is done by host.

7. Interface

7.1. Pad Assignment

Pad	Name	Pad Description	Direction	Full Power	Hibernate	Notes
1	GND	System Ground	Power			
2	RF_IN	Antenna Signal Input	Input			
3	GND	System Ground	Power			
4	WAKEUP	Power Status	Output	High	Low	
5	nRESET	Asynchronous Reset	Input	High	High	Internal pull-up
6	nCTS	UART CTS / SPI CLK	Bi-dir.	Low	Low	Internal pull-down
7	nRTS	UART RTS / SPI nCS	Bi-dir.	High	High	Internal pull-up
8	RX	UART RX / SPI MOSI / I^2C SDA	Bi-dir.	High	Hi-Z	
9	ON_OFF	Power State Control	Input	Low	Low	Schmitt-triggered input
10	1PPS	UTC Time Mark	Output	Low	Low	
11	TX	UART TX / SPI MISO / I^2C SCL	Bi-dir.	Low	Hi-Z	
12	V_{CC}	System Power	Power			
13	RTC	Future use				Do not connect
14	GND	System Ground	Power			
15	DR_SDA	DR I^2C Serial Data	Output		Hi-Z	Do not connect
16	DR_SCL	DR I^2C Serial Clock	Bi-dir.		Hi-Z	Do not connect

Table 7-1: Pin-out

7.2. Connectivity

7.2.1. Power

Power supply

ORG4472 module requires only one power supply V_{CC} of 1.8V DC.
It is recommended to keep the power supply on all the time in order to maintain the non-volatile RTC and RAM active for fastest possible TTFF.
When powering ORG4472 module from switching mode (DC-DC) power supply carefully follow manufacturer's application notes and apply filtering to minimize ripple.
Voltage ripple below 300mV$_{PP}$ allowed for frequency under 10KHz.
Voltage ripple below 100mV$_{PP}$ allowed for frequency between 10KHz and 100KHz.
Voltage ripple below 50mV$_{PP}$ allowed for frequency between 100KHz and 1MHz.
Voltage ripple below 10mV$_{PP}$ allowed for frequency above 1MHz.
Higher voltage ripple may compromise the ORG4472 module performance.
When the V_{CC} is powered off settings are reset to factory default and the receiver performs Cold Start on next power up.
Power supply current varies according to the processor load and satellite acquisition.
Typical I_{CC} current is 40mA during acquisition. Peak I_{CC} current is 55mA.
Typical I_{CC} current in Hibernate state is 20µA.

Ground

All Ground pads should be connected to the main Ground plane with shortest possible traces or vias.

7.2.2. Host Control Interface

ON OFF control input

The ON_OFF control input can be used to switch the receiver between Normal or Hibernate states and also to generate interrupt in PTF™ mode.
The ON_OFF interrupt is generated by a low-high-low toggle, which should be longer than 62µs and less than 1s (100ms pulse length recommended).
ON_OFF interrupts with less than 1 sec intervals are not recommended.
Multiple switch bounce pulses are recommended to be filtered out.
ON_OFF input is 3.6V tolerant.
Pull-down resistor of 33kΩ-82kΩ is recommended.
Must be connected to host.

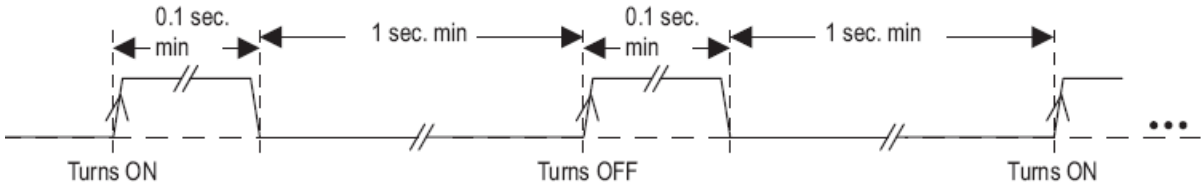


Figure 7-1: ON_OFF timing

nRESET input

The Power-on-Reset (POR) is generated internally in the ORG4472 module.
Additionally, manual reset option is available through nRESET pad.
Resetting the module clears the RTC block and configuration settings become default.
nRESET pad is active low and has internal pull-up resistor of 86kΩ (typ.).
nRESET signal should be applied for at least 1µs.
Do not drive nRESET input high.
Do not connect if not in use.

WAKEUP output

The WAKEUP pad is an output from the ORG4472 module, used to flag for power mode.
A low on this output indicates that the module is in one of its low-power states - Hibernate or Standby.
A high on this output indicates that the module is in Full Power operating mode.
WAKEUP output can be used to control enable of auxiliary devices, like level translator, active antenna bias, or to flag for high current demand from power supply.
Wakeup output is LVCMOS 1.8V compatible.

1PPS output

The pulse-per-second (PPS) output provides a pulse signal for timing purposes.
Pulse length (high state) is 200ms, and less than 1µs synchronized to full UTC second.
The UTC time message is generated and put into output FIFO 300ms after PPS rising edge.
The exact time between the PPS and UTC time message delivery depends on message rate, message queue and communication baud rate.
1PPS output is LVCMOS 1.8V compatible.
Do not connect if not in use.

7.2.3. Host Data Interface

ORG4472 module has 3 types of interface ports to connect to host: UART, SPI and I^2C.
All ports are multiplexed on a shared set of pads.
At system reset, the host port interface lines are disabled, so no conflict occurs.
Configuration straps on nCTS and nRTS are read by the module firmware during startup and define port type. Use 10kΩ resistor for external strap.

Port Type	nCTS	nRTS
UART	External pull-up	Don't install an external pull up
SPI (default)	Don't install an external pull up	Don't install an external pull up
I^2C	Don't install an external pull up	External pull-down

Table 7-2: ORG4472 host interface selection

UART

The module has a 4-wire UART port:

- TX used for GPS data reports.
- RX used for receiver control.
- nCTS and nRTS are optionally used for hardware flow control.

The default protocol is NMEA@4,800bps 8-N-1 (8 data bits, No parity, 1 stop bit).
The configuration for baud rates and respective protocols can be changed by commands via NMEA or OSP (SiRF Binary) protocols. Baud rates are configurable from 900bps to 1.8Mbps.

Baud Rate (bps)	Error (%)
900	0.00
1200	0.00
1800	0.00
2400	0.00
3600	0.00
4800	0.06
7200	0.00
9600	0.00

Baud Rate (bps)	Error (%)
14400	0.62
19200	0.00
28800	0.00
38400	0.07
57600	0.64
76800	0.01
115200	0.24
153600	0.03

Baud Rate (bps)	Error (%)
230400	1.04
307200	0.01
460800	0.60
614400	1.10
921600	2.30
1228800	0.07
1843200	0.86

Table 7-3: ORG4472 UART baud rate tolerance

Outputs are LVCMOS 1.8V compatible. Inputs are 3.6V tolerant.

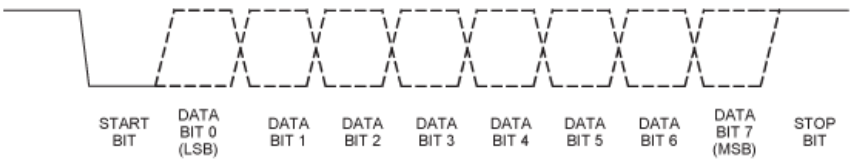


Figure 7-2: UART integrity

SPI

The SPI (Serial to Peripheral Interface) is a master/slave synchronous serial bus that consists of 4 signals:

- Serial Clock (SCK) from master to slave.
- Serial Data Out (also called Master Out Slave In or MOSI) from master.
- Serial Data In (also called Master In Slave Out or MISO) from slave.
- Chip Select (CS) from master.

The host interface SPI of the ORG4472 module is a slave mode SPI.
The four SPI pads are RX (MOSI), TX (MISO), nRTS(nCS) and nCTS(SCK).
Output is LVCMOS 1.8V compatible. Inputs are 3.6V tolerant.
The host interface SPI features are:

- TX and RX each have independent 1024 byte FIFO buffers.
- RX and TX have independent, software specified two byte idle patterns of 0xA7 0xB4.
- TX FIFO is disabled when empty and transmits its idle pattern until re-enabled.
- RX FIFO detects a software specified number of idle pattern repeats and then disables FIFO input until the idle pattern is broken.
- FIFO buffers can generate an interrupt at any fill level.
- SPI detects synchronization errors and can be reset by software.
- Supports a maximum clock of 6.8MHz.
- Default GPS data output format is NMEA standard.

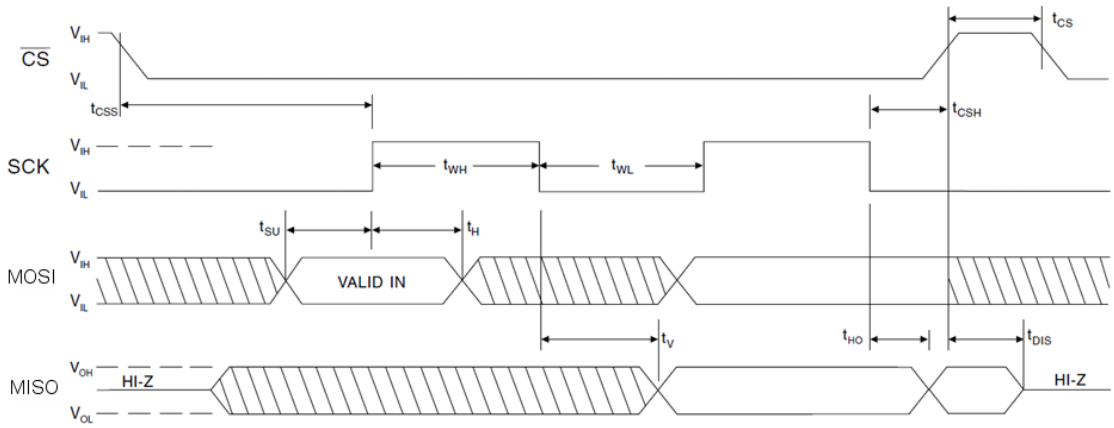


Figure 7-3: SPI timing

Symbol	Parameter	Min	Max	Units
t_{CLK}	SCK Time Period	140		ns
t_{CSS}	nCS Setup Time	0.5	1	t_{CLK}
t_{CS}	nCS High Time	1		t_{CLK}
t_{WH}	SCK High Time	0.5		t_{CLK}
t_{WL}	SCK Low Time	0.5		t_{CLK}
t_{CSH}	nCS Hold Time	0.5	1	t_{CLK}
t_{SU}	Data In Setup Time	0.5		t_{CLK}
t_H	Data In Hold Time	0.5		t_{CLK}
t_V	Output Valid	0.5		t_{CLK}
t_{HO}	Output Hold Time	0.5		t_{CLK}
t_{DIS}	Output Disable Time		0.5	t_{CLK}

Table 7-4: SPI timing

Operation:

The SPI performs bit-by-bit transmitting and receiving at the same time whenever nCS is asserted and SCK is active. In order to communicate properly with SPI device, the protocol must be agreed – specifically- SPI mode and an idle byte pattern.

Among 4 SPI modes of the clock polarity (CPOL) and clock phase (CPHA) only SPI Mode 1 <CPOL="0", CPHA ="1"> has been tested:

- At CPOL="0" the base value of the clock is zero.
- For CPHA="1", data are read on the clock's falling edge and data are changed on a rising edge.

On power up, the first message to come out of the module is the "OK_TO_SEND" message.

It takes about 20ms from power up for the module SPI drivers to get initialized.

The slave has no way of forcing data to the master to indicate it is ready for transmission - the master must poll the client periodically.

Since the specified idle 2-byte pattern for both receive and transmit is 0xA7 0xB4, the master can transmit this idle pattern into the slave repeatedly. If the master receives idle patterns back from the slave, it indicates that the slave currently has nothing to transmit but is ready to communicate.

On the module receive side, the host is expected to transmit idle pattern when it is querying the module's transmit buffer. In this way, the volume of discarded bytes is kept nearly as low as in the UART implementation because the module hardware does not place most idle pattern bytes in its RX FIFO. Most messaging can be serviced with polling. The FIFO thresholds are placed to detect large messages requiring interrupt-driven servicing.

On the module transmit side the intent is to fill the FIFO only when it is disabled and empty. In this condition, the module's SPI driver software loads as many queued messages as can completely fit in the FIFO. Then the FIFO is enabled.

The host is required to poll messages until idle pattern bytes are detected.

At this point the module's FIFO is empty and disabled, allowing the ORG4472 SPI driver to again respond to an empty FIFO interrupt and load the FIFO with any messages in queue.

Notes:

For SPI communication, read and write operations both require data being sent to the Slave SPI (idle bytes for reads and message data for writes). Any time data is sent to the module via the SPI bus, the Slave SPI of the module will send an equal amount of data back to the host.

These bytes must be buffered either in hardware or software, and it is up to the host to determine if the bytes received may be safely discarded (idle bytes), or should be passed on to the application handling GPS communication. Failure to properly handle data received from the SPI slave can result in corrupted GPS messages.

The external SPI master may send idle bytes and complete messages in a single transmission, provided that idle bytes shall not be inserted inside of a message.

The idle byte pattern and repeat count prevents the problem of messages lost due to normal occurrence of idle byte patterns within message data with high probability.

The external SPI master shall not send partial messages.

All transmissions from the SPI master shall be in multiples of 8 bits.

The external SPI master shall transmit the idle byte pattern when reading the SPI slave's transmit buffer when the master has no message data to transmit.

The SPI slave shall be serviced at a rate that will keep the TX FIFO empty.

ORG4472

I²C

I²C is a low- to medium-data-rate master/slave communication bus.
Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus. At that time, any device addressed is considered a slave.
The physical layer of I²C bus is a simple handshaking protocol that relies upon open collector outputs on the bus devices and the device driving or releasing the bus lines, so a pull-up resistor is needed on each wire of the bus.
I²C bus is a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer
Serial 8-bit oriented bi-directional data transfers can be made at up to 100kbps in the Standard-mode of I²C bus and up to 400kbps in the Fast-mode.
The Host Interface I²C features are:

- Multi-Master I²C mode is supported by default.
- Individual transmit and receive FIFO length of 64 bytes.
- The default I²C address values are:
  - RX: 0x60
  - TX: 0x62
- Operation speed up to 400kbps.
- SCL and SDA require external pull-up resistors of 2.2kΩ (typ.).

Operation:

The operation of the I²C with a master transmit and slave receive mimics a UART operation, where both the module and the host can independently freely transmit.
It is possible to enable the master transmit and slave receive at the same time, as the I²C bus allows for contention resolution between the module and the host vying for the bus.

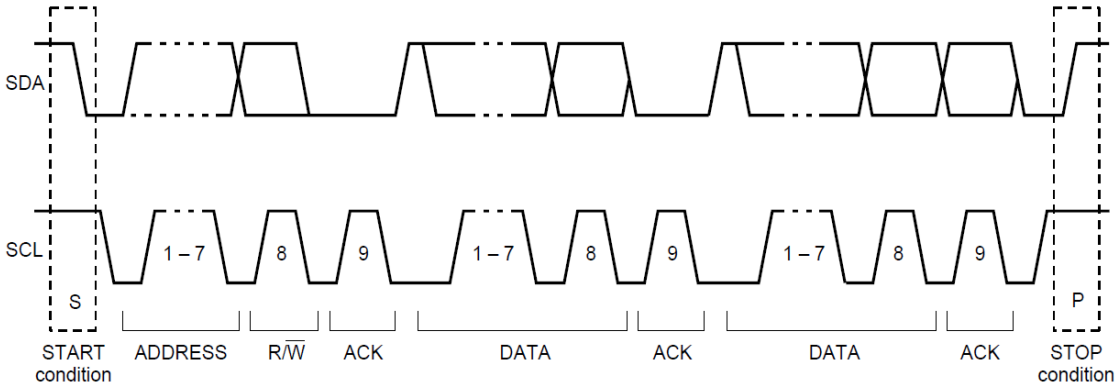


Figure 7-4: I²C integrity

Figure 7-3 shows typical data transfers on the I²C bus. The master supplies the clock; it initiates and terminates transactions and the intended slave (based upon the address provided by the master) acknowledges the master by driving or releasing the bus. The slave cannot terminate the transaction but can indicate a desire to by a “NAK” or not-acknowledge.

I²C specification defines unique situations as START (S) and STOP (P) conditions.
A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition.
A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.
START and STOP conditions are always generated by the master.
Every byte put on the SDA line must be 8-bits long.
The number of bytes can be transmitted per transfer is unrestricted.
Each byte is followed by an acknowledge bit.
Data is transferred with the Most Significant Bit (MSB) first. In most cases, data transfer with acknowledge is obligatory. The acknowledge–related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. Set-up and hold times must be taken into account.
All data transfers of I²C specification should follow the format.
After the START condition (S), a slave address should be sent first.
This address is 7 bits long followed by an 8-th bit which is a data direction bit (R/nW) – logical 0 indicates a transmission (WRITE), logical 1 indicates a request for data (READ).
After the slave address byte is sent, master can continue its data transfer by writing or reading data byte as defined format. The data transfer is always terminated by a STOP condition generated by the master.

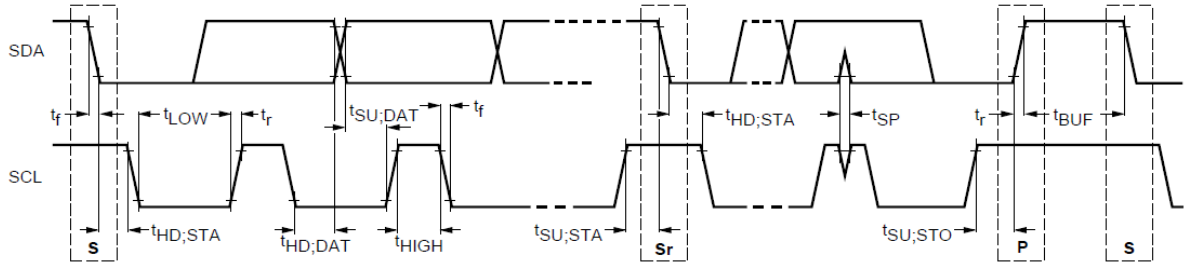


Figure 7-5: I²C timing

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL frequency	100	400	kHz
$t_{HD;STA}$	Hold Time for START condition	0.6		µs
t_{LOW}	Low Time of SCL	1.3		µs
t_{HIGH}	High Time of SCL	0.6		µs
$t_{SU;STA}$	Setup Time for START condition	0.6		µs
$t_{HD;DAT}$	Hold Time	0	0.9	µs
$t_{SU;DAT}$	Data Setup Time	0.1		µs
t_r	Rise Time of SDA and SCL		0.3	µs
t_f	Fall Time of SDA and SCL		0.3	µs
$t_{SU;STO}$	Setup Time for STOP condition	0.6		µs
t_{BUF}	Bus Free Time between START and STOP	1.3		µs
C_L	Capacitive Load of SDA and SCL		400	pF
V_{nL}	Noise Margin at the low logic level		$0.1 \cdot V_{CC}$	V
V_{nH}	Noise Margin at the high logic level		$0.2 \cdot V_{CC}$	V

Table 7-5: I²C timing

7.2.4. Smart Sensors Data Interface

ORG4472 master mode I²C auxiliary interface provides support for dead reckoning (DR) and code patch upload (optional).
The port has 2 pads, DR_SCL and DR_SDA, both pins are pseudo open-drain and require pull-up resistors on the external bus.

Dead Reckoning (DR) I²C Interface

The DR I²C interface supports required sensor instruments for dead reckoning applications such as gyros, accelerometers, compasses or other sensors that can operate with an I²C bus. ORG4472 module acts as the I²C Master and the sensor devices function in Slave mode. This provides a very low latency data pipe for the critical sensor data so that it can be used in the Navigation Library and Kalman filter to enhance navigation performance.
The MEMS algorithms perform a sensor data fusion with the GPS signal measurements. GPS measurements can be used to calibrate the MEMS sensors during periods of GPS navigation. The MEMS sensors can augment GPS measurements, and can be more accurate than GPS under degraded GPS signal conditions and certain dynamics.
DR I²C interface supports:

- Common sensor formats
- Typical data lengths (command + in/data out) of several bytes
- Standard I²C bus maximum data rate 400kbps
- Minimum data rate 100kbps

In current firmware implementation MEMS sensors integration provides a pseudo “position pinning” feature to prevent position wander and heading instability.

Data Storage Support

The DR I²C interface is available at boot-up for uploading data from a serial EEPROM. Firmware updates may be provided from time to time to address ROM firmware issues as a method of performance improvement.
The DR I²C interface also supports serial flash devices used to store ARM7TDMI patch loads, including optional:

- FIFO support
- ARM7TDMI dedication to I²C interface during serial flash read or write

7.2.5. RF input

The antenna input impedance is 50Ω. The input is DC blocked.
The module supports active and passive antennas.
In design with passive antenna attention should be paid on antenna layout.
Short trace with controlled impedance of 50Ω should conduct GPS signal from antenna to RF_IN pad.
In designs with active antenna DC bias voltage should be applied on RF_IN through AC blocking inductor. DC bias voltage can be controlled by WAKEUP output through MOSFET or load switch.
In designs with active antenna net gain including conductors losses should not exceed 25dB.
In designs with external LNA, LNA enable input can be controlled by the ORG4472 WAKEUP output.

7.3. Typical Application Circuit

7.3.1. Minimal Schematic Diagrams with passive antenna

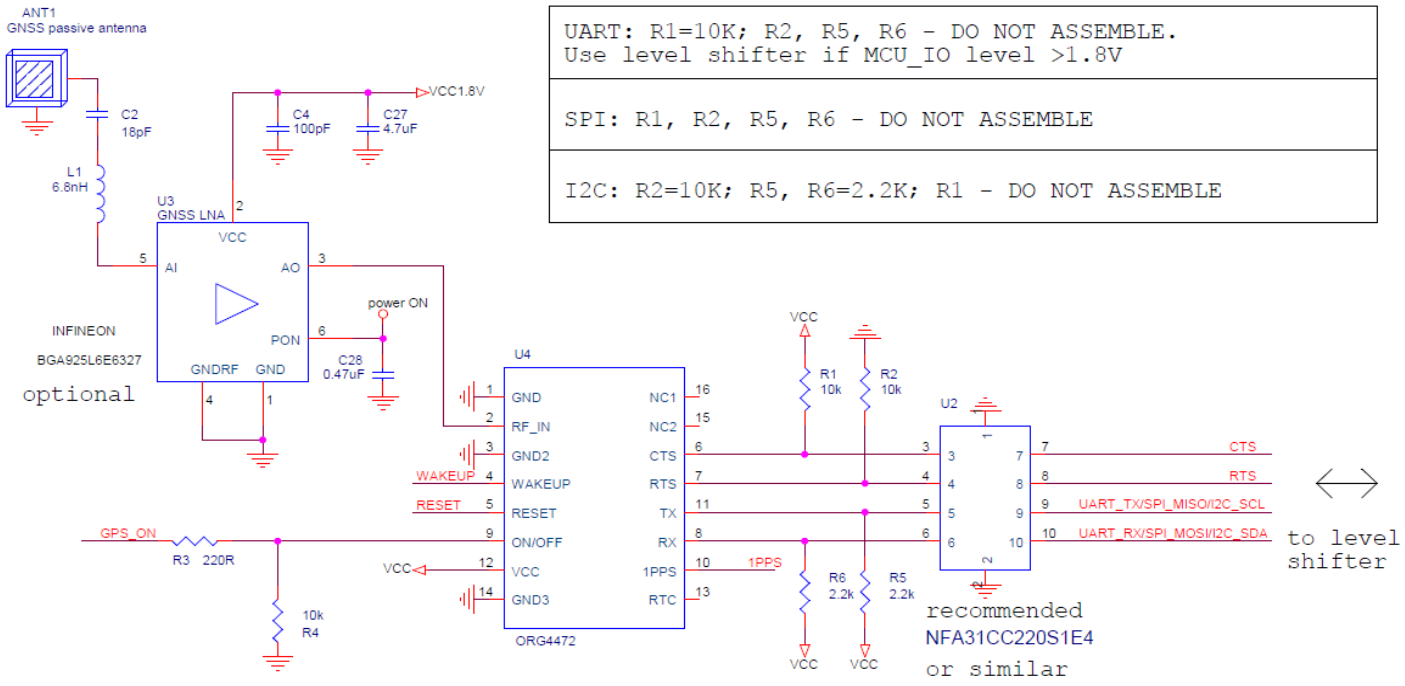


Figure 7-6: Typical application circuit

7.3.2. Extended Schematic Diagrams with active antenna

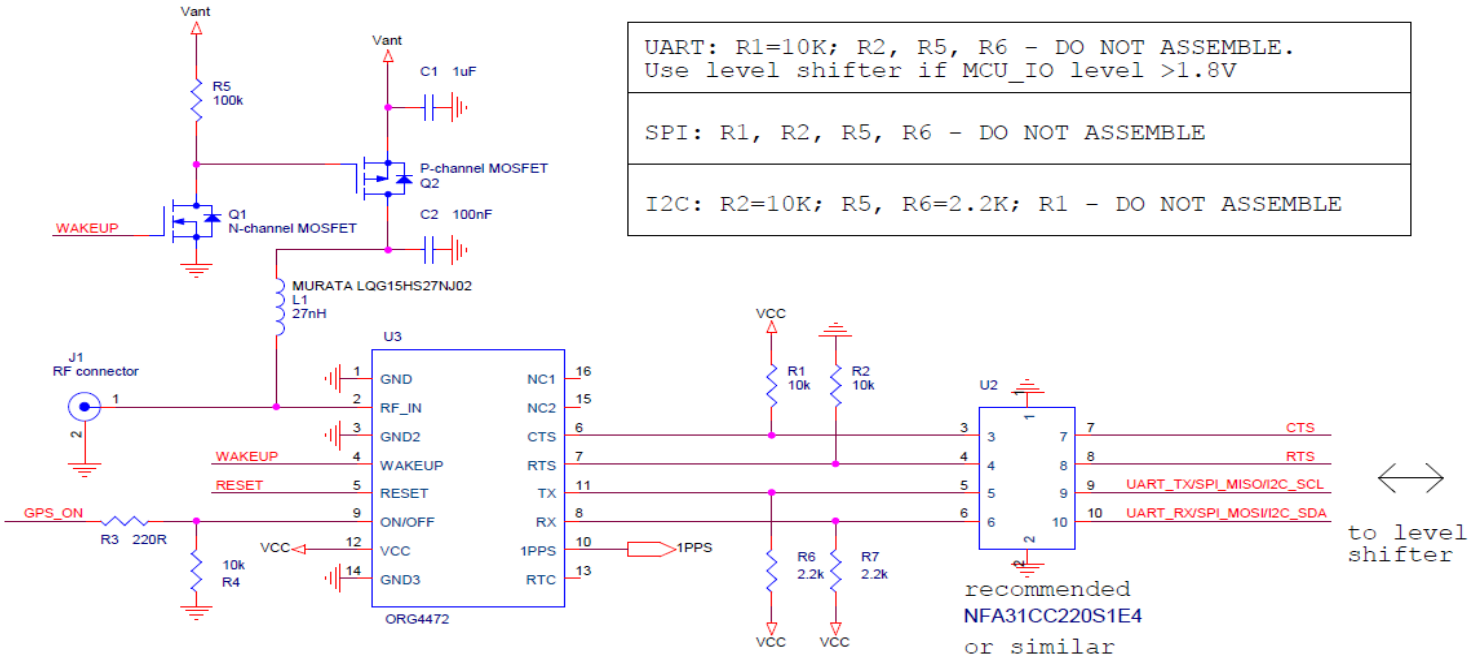


Figure 7-10: Active Antenna and UART interface circuit

8. PCB Layout

8.1. Footprint

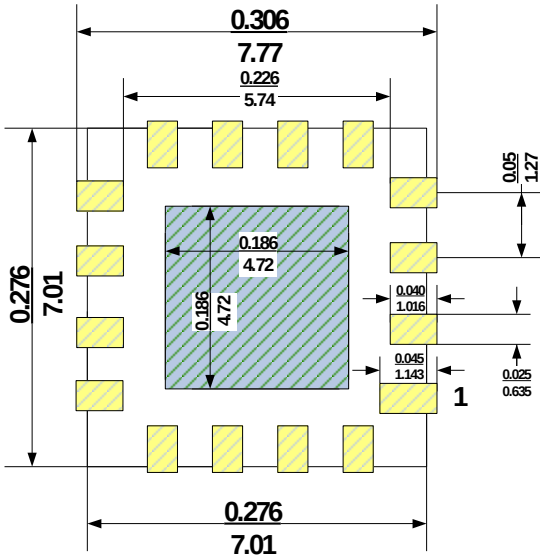


Figure 8-1: Footprint $\frac{\text{inch}}{\text{millimeter}}$

Ground pad at the middle should be connected to main Ground plane by multiple vias.
Ground pad at the middle should be solder masked.
Silk print of module's outline is highly recommended for SMT visual inspection.

8.2. RF Input trace

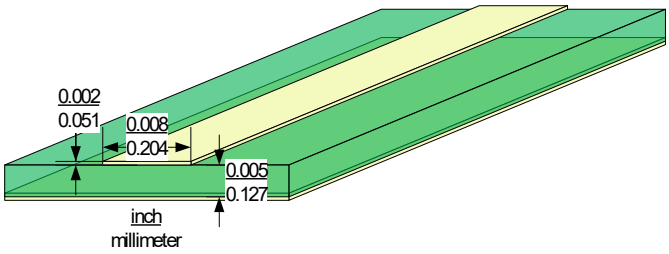


Figure 8-2: Typical Microstrip PCB trace on FR-4 substrate

8.3. PCB stack up

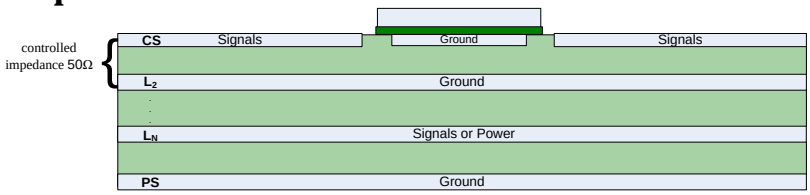


Figure 8-3: Typical PCB stack up

8.4. Design restrictions

Keep out of signal or switching power traces and vias under the ORG4472 module.
Signal traces to/from ORG4472 module should have minimum length.
Recommended distance from adjacent active components is 3mm. In case of adjacent high speed components, like CPU or memory, high frequency components, like transmitters, clock resonators or oscillators, metal planes, like LCD or battery enclosures, please contact OriginGPS for more precise, application specific recommendations.

9. Operation

When power is first applied, the ORG4472 goes into a Hibernate state while integrated RTC starts and internal FSM sequences though to “Ready-to-Start” state.

The host is not required to control external master nRESET since module’s internal reset circuitry handles detection of application of power.

While in “Ready-to-Start” state, the module awaits a pulse to the ON_OFF input.

Since integrated RTC startup times are variable, detection of when the ORG4472 is ready to accept an ON_OFF pulse requires the host to either wait for a fixed interval, to monitor a pulse on module WAKEUP output that indicates FSM “Ready-to-Start”

Another option is to assert a pulse on the ON_OFF input every second until the ORG4472 module starts by indicating a high on WAKEUP or generation of UART messages.

9.1. Starting the ORG4472 module

A pulse on the ON_OFF input line when ORG4472 FSM is ready and in startup-ready state, Hibernate state, standby state, will command the module to start.

ON_OFF pulse requires a rising edge and high level that persists for at least 100 µs in order to be detected. Resetting the ON_OFF detector requires that ON_OFF go to logic low at least 100 µs.

- If the system is in Hibernate state, an ON_OFF pulse will move to Full Power mode
- If the system is in Trickle Power Mode, an ON_OFF pulse will move it to Full Power mode.
- If the system is in Push-To-Fix mode, an ON_OFF pulse will initiate one Push-To-Fix cycle.
- If the system is already in Full Power mode, an ON_OFF pulse will initiate orderly shutdown.

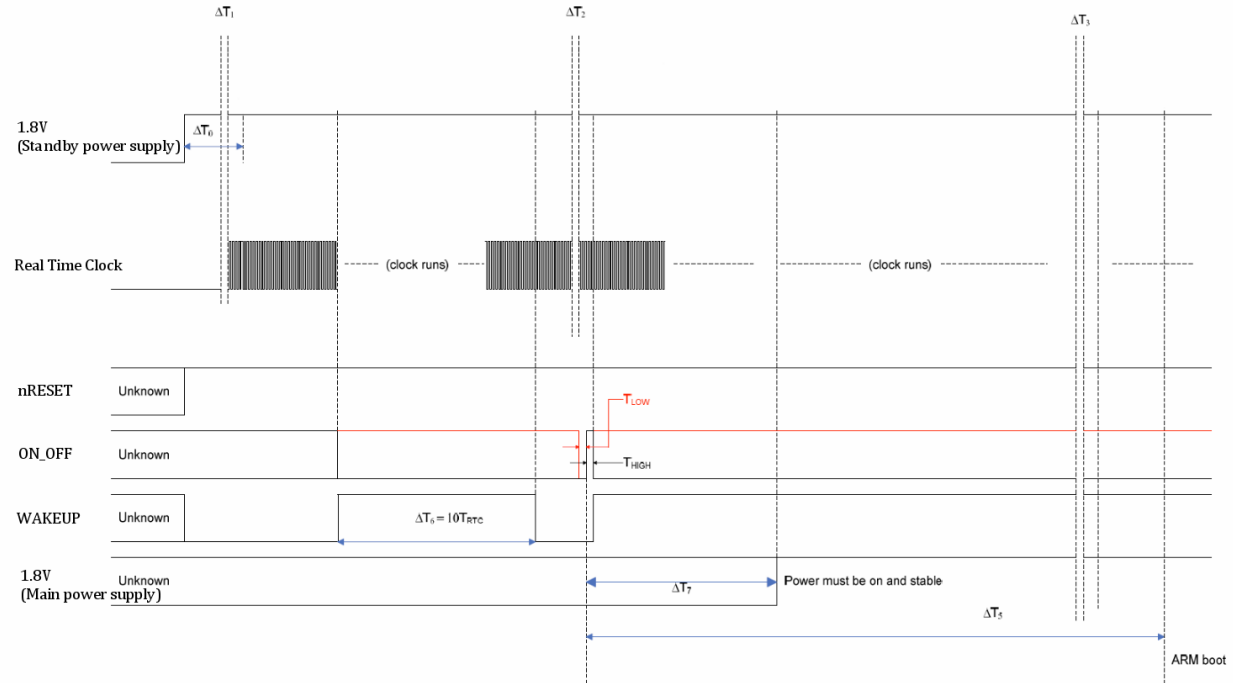


Figure 9-1: Startup timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{RTC}	RTC frequency	25^0C	-20 ppm	32768	+20 ppm	Hz
t_{RTC}	RTC tick	25^0C		30.5176		µs
ΔT_1	RTC startup time			300		ms
ΔT_0	Power stabilization		$6 \cdot t_{RTC}+\Delta T_1$	$7 \cdot t_{RTC}+\Delta T_1$	$8 \cdot t_{RTC}+\Delta T_1$	µs
ΔT_6	WAKEUP pulse	RTC running		10		t_{RTC}
ΔT_{LOW}	ON_OFF low		3			t_{RTC}
ΔT_{HIGH}	ON_OFF high		3			t_{RTC}
ΔT_3	Startup sequencing	After ON_OFF		1024		t_{RTC}
-	ON_OFF to WAKEUP high	After ON_OFF		6		t_{RTC}
ΔT_5	ON_OFF to ARM start	After ON_OFF		2130		t_{RTC}
ΔT_7	Main power source start[1]	WAKEUP high	0	30	300	t_{RTC}

Table 9-1: Startup timing

Note:
1. When power provided through dual supply.
Low quescent current 1.8V source (LDO) for Hibernate state, and high efficiency 1.8V source (DC-DC) for Full Power state.
The main power supply should be able to provide current for Full Power state within 1ms after WAKEUP is high.

9.2. Verifying the ORG4472 module has started

The ORG4472 module WAKEUP output will go high indicating the internal processor has started.
System activity indication depends upon the serial interface chosen.
UART:
- With no flow control - when active, the module will output NMEA messages at the 4800bps.
- With flow control - nCTS must be released by host to allow the module to send messages.

I^2C:
- In Multi-Master mode with no bus contention - the module will spontaneously send messages at the speed and message types selected.
- In Multi-Master mode with bus contention - the module will send messages after the I^2C bus contention resolution process allows it to send.

SPI:
- Since the module is SPI slave, there is no possible indication of system “ready” through SPI interface.
- The host must initiate SPI connection approximately one second after WAKEUP goes high.

9.3. Shutting down the ORG4472 module

Transferring the ORG4472 module into Hibernate mode can be initiated in two ways:
- By a pulse on the ON_OFF input when the ORG4472 module in Full Power mode
- By serial messages in OSP (MID205) or NMEA ($PSRF117)

The orderly shutdown may take anywhere from 10ms to 900ms to complete, depending upon operation in progress and messages pending, and hence is dependent upon serial interface speed and controls.

10.Software Functions

The module supports NMEA-0183 ASCII protocol and One Socket Protocol (based on SiRF Binary Standard).

Power On State		Full Power
Default Interface[1]		UART
SPI data format		NMEA
UART data format		NMEA
UART settings		4,800 bps 8-N-1
I^2C data format		NMEA
NMEA Messages		$GPGGA @1 sec.
		$GPGSA @ 1 sec.
		$GPGSV @ 5 sec.
		$GPRMC @ 1 sec.
Firmware features	SBAS	OFF
	ABP	OFF
	Static Filter	OFF
	Track Smoothing	OFF
	Internal DR	OFF
	Low Power	OFF
	Update rate	1Hz (configurable up to 5Hz)

Table 10-1: Operation defaults

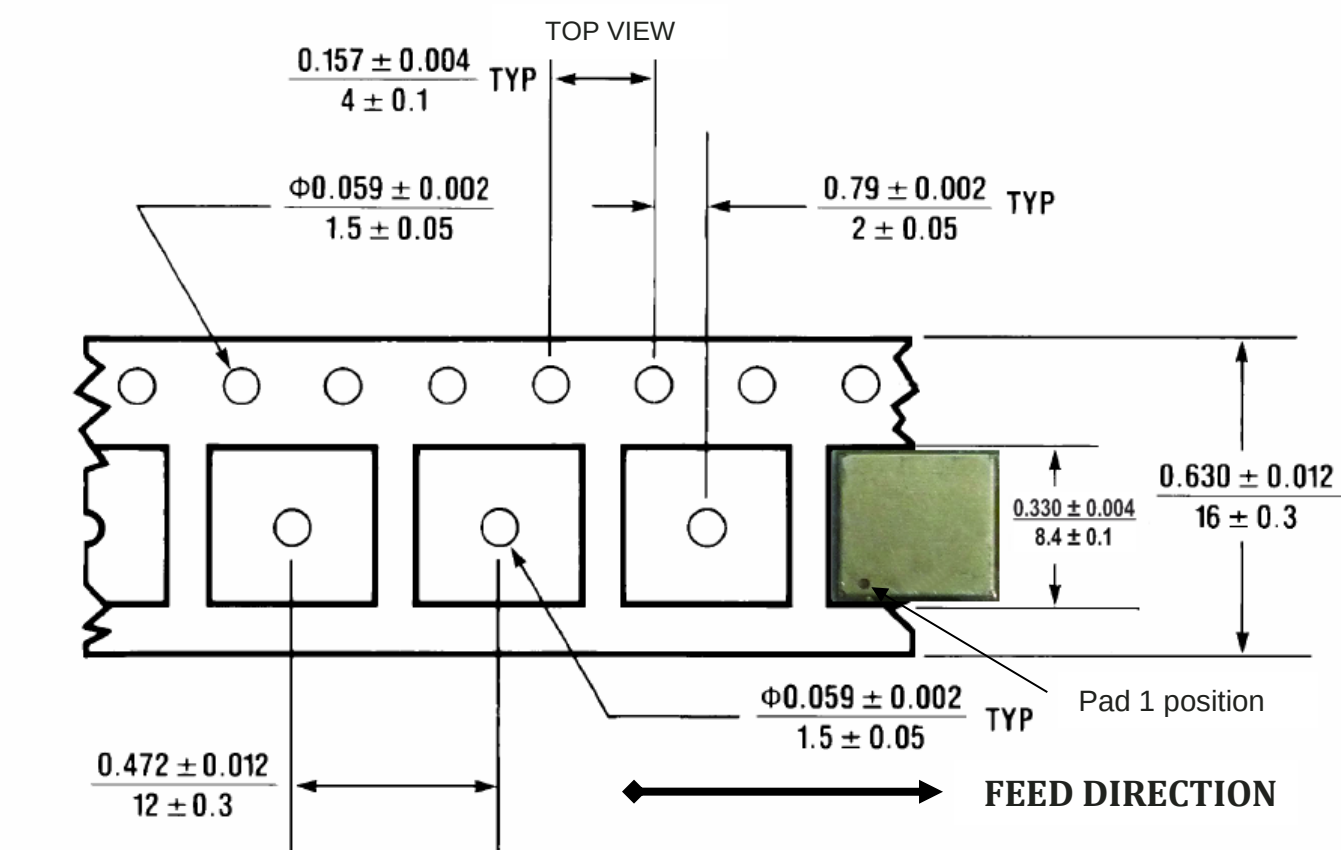
Notes:
1. Without Pull-Up on nCTS or Pull-Down on nRTS.

10.1. Firmware Update

Firmware updates can be considered exclusively as patches on top of baseline ROM firmware.
Those patch updates may be provided from time to time to address ROM firmware issues as a method of performance improvement. Typical patch file size is 24KB.
Host controller is initiating load and application of patch update by communicating module's Patch Manager software block allocating 16KB of memory space for patch and additional 8KB for cache.
Patch updates are preserved until BBRAM is discarded.
Upgrading the Patch is mandatory for stable operation.

11.Handling Information

11.1. Product Packaging and Delivery



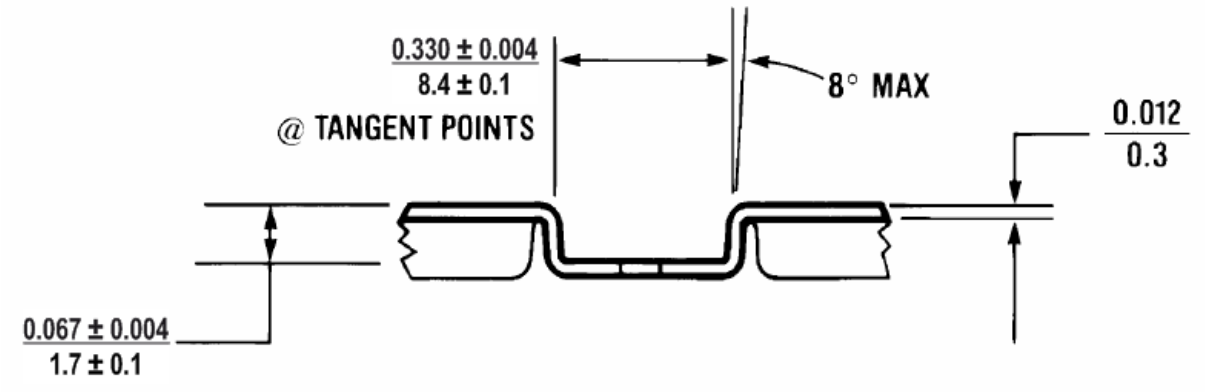


Figure 11-1: Carrier $\frac{\text{inch}}{\text{millimeter}}$

Carrier material: Conductive Polystyrene

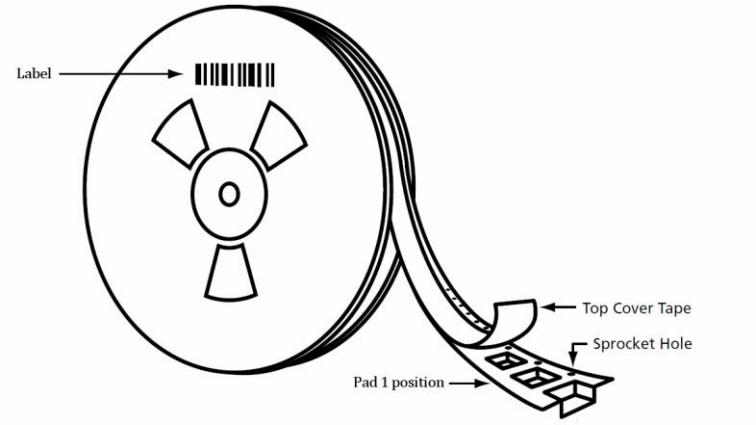


Figure 11-2: Module position

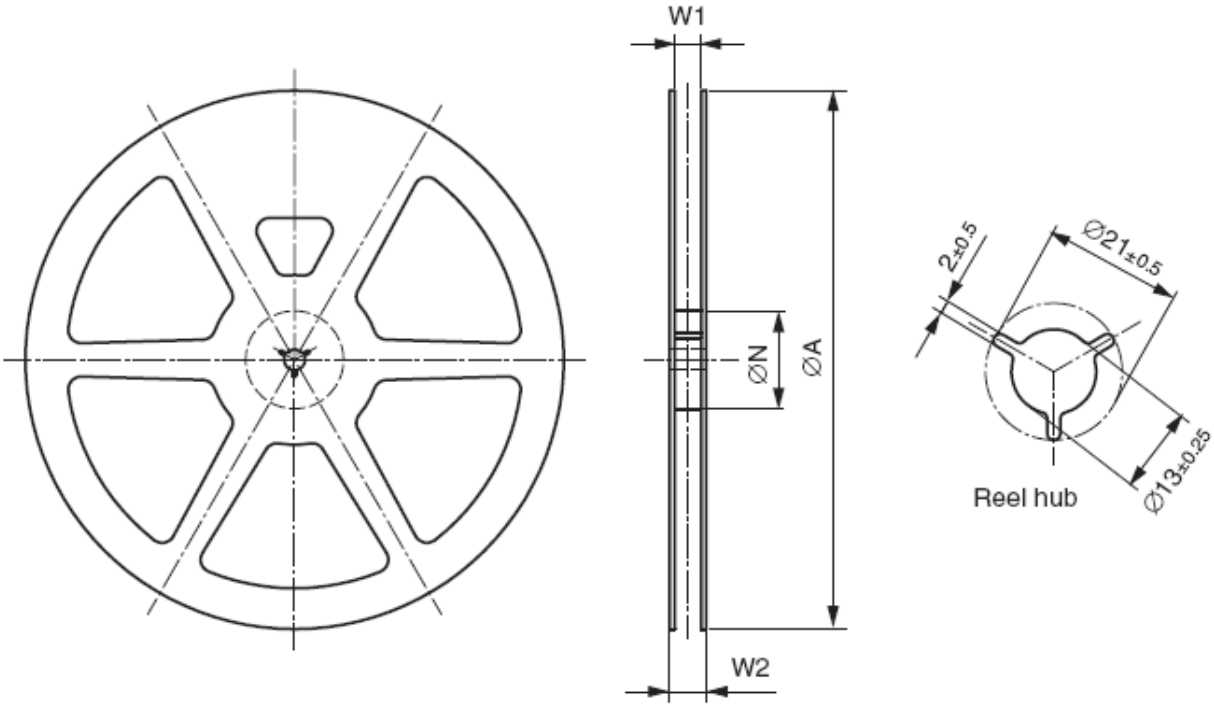


Figure 11-3: Reel

Reel Des.	TR1		TR2	
	mm	inch	mm	inch
ØA	178 ± 1	7.00 ± 0.04	330 ± 2	13.00 ± 0.08
ØN	60 ± 1	2.36 ± 0.04	102 ± 2	4.02 ± 0.08
W_1	16.7 ± 0.5	0.66 ± 0.02	16.7 ± 0.5	0.66 ± 0.02
W_2	19.8 ± 0.5	0.78 ± 0.02	22.2 ± 0.5	0.87 ± 0.02

Table 11-2: Reel dimensions [mm]

Reel material: Antistatic Plastic.

Units per reel	TR1	TR2
Standard	500	2000

Table 11-3: Reel quantity

11.2. Moisture Sensitivity

The devices are moisture sensitive at MSL 3 according to standard IPC/JEDEC J-STD-033B.

The recommended drying process for samples and bulk components is to be done at 125°C for 48 hours.

11.3. Assembly

The ORG4472 module support automatic assembly and reflow soldering processes on the component side of the motherboard PCB according to standard IPC/JEDEC J-STD-020D for LGA SMD. Suggested solder paste stencil is 5 mil to ensure sufficient solder volume.

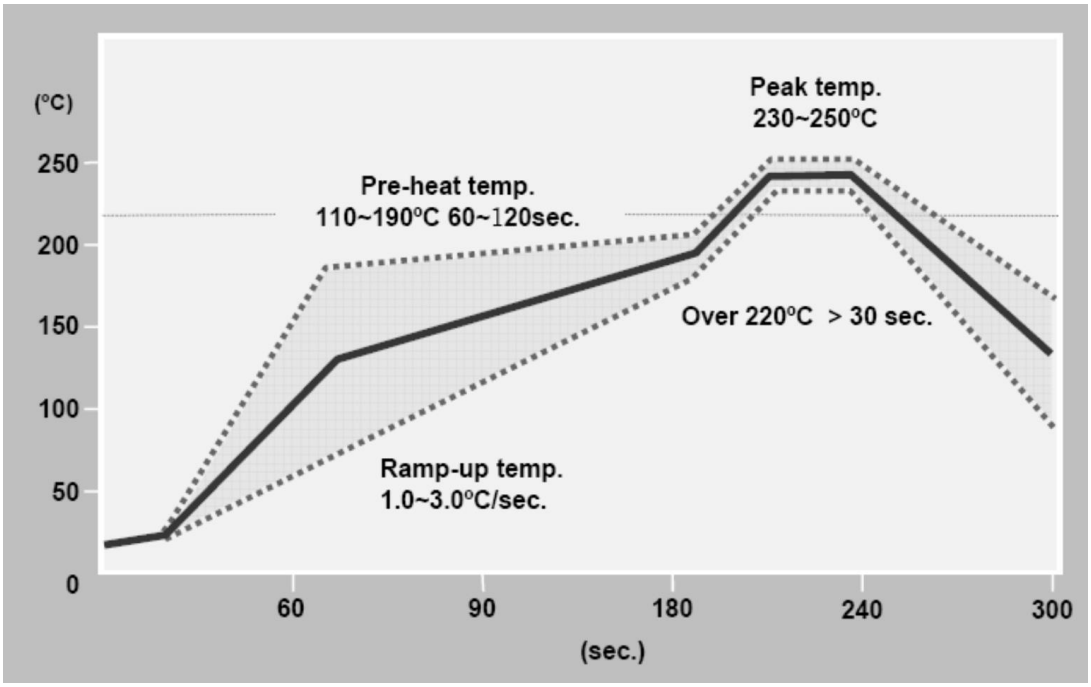


Figure 11-4: Recommended soldering profile

Suggested peak reflow temperature is 250°C for 10 sec. for Pb-Free solder paste.

Absolute Maximum reflow temperature is 260°C for 10 sec.

11.4. Rework

If localized heating is required to rework or repair the ORG4472 module, precautionary methods are required to avoid exposure to solder reflow temperatures that can result in permanent damage to the device.

11.5. ESD Sensitivity

The ORG4472 module is ESD sensitive device and should be handled with care.

11.6. Compliances

The following standards are applied on the ORG4472 modules production:

- IPC-6011/6012 Class2 for PCB manufacturing
- IPC-A-600 Class2 for PCB inspection
- IPC-A-610D Class2 for SMT acceptability

ORG4472 modules are being manufactured ISO 9001:2000 accredited facilities.

ORG4472 modules are designed and being manufactured and handled to comply with and according with Pb-Free/RoHS Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

The ORG4472 modules comply with the following EMC standards:

- EU CE EN55022:06+A1(07), Class B
- US FCC 47CFR Part 15:09, Subpart B, Class B

11.7. Safety Information

Improper handling and use can cause permanent damage to the device.

There is also the possible risk of personal injury from mechanical trauma or shocking hazard.

11.8. Disposal Information

The product should not be treated as household waste.

For more detailed information about recycling electronic components, please contact your local waste management authority.

12.Mechanical Specifications

- ORG4472 module has advanced ultra-miniature packaging and a LGA SMD footprint.
- ORG4472 module's PCB footprint size is 7mm x 7mm
- ORG4472 module is surface mount device packaged on a miniature printed circuit board with a metallic RF enclosure on top of it.
- There are 16 surface mount connection pads with a base metal of copper and an Electroless Nickel / Immersion Gold (ENIG) finish.
- ORG4472 module was designed and packaged for automated pick and place assembly and reflow soldering processes.

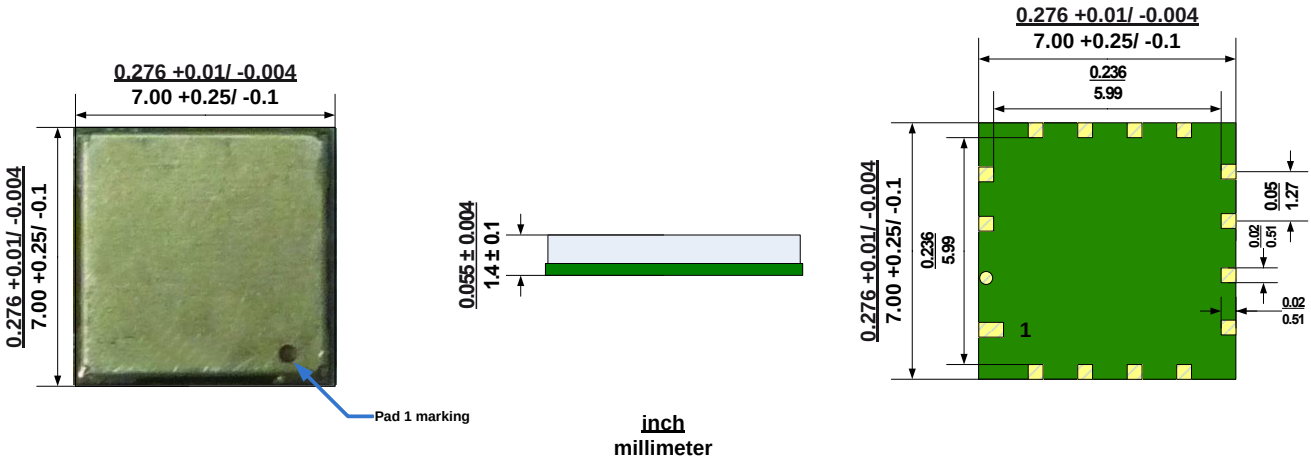


Figure 12-1: ORG4472 mechanical drawing

Dimensions	Length	Width	Height	Weight	
mm	7.0 +0.25/ -0.1	7.0 +0.25/ -0.1	1.4 ± 0.1	gr	0.3
inch	0.276 +0.01/ -0.004	0.276 +0.01/ -0.004	0.055 ± 0.004	oz	0.05

Table 12-1: ORG4472 mechanical summary

13.Ordering Information

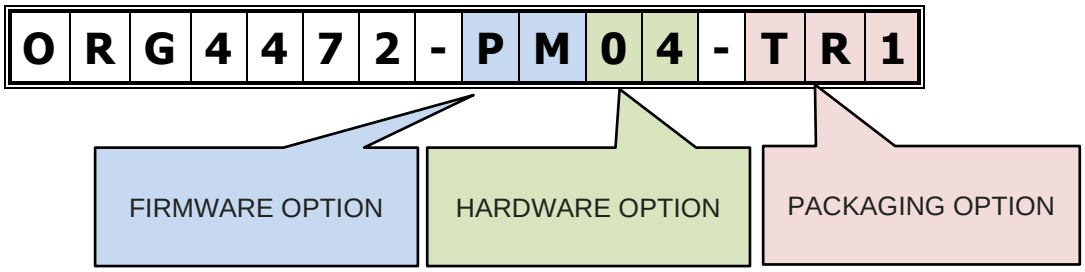


Table 13-1: Ordering options

PART NUMBER	FW VERSION	HW OPTION	Vcc RANGE	PACKAGING	SPQ
ORG4472-PM04-TR1	PM	04	1.8V	REELED TAPE	500
ORG4472-PM04-TR2	PM	04	1.8V	REELED TAPE	2000
ORG4472-PM04-UAR	PM	04	5V	EVALUATION KIT	1

Table 13-2: Orderable devices

14. I2C Appendix

I²C host interface features are:

- I²C Multi-Master mode - module initiates clock and data, default operating speed 400kbps.
- I²C address '0x60' for commands from controller to GPS-module. (Default)
- I²C address '0x62' for the data transmits from the GPS-module to the host. (Default)
- Individual transmit and receive FIFO length of 64 bytes.
- SCL and SDA are pseudo open-drain lines, therefore require external pull-up resistors of 2.2kΩ to 1.8V, or 3.3kΩ to 3.3V.
- Multi-Master mode – the Host (MCU) can operate either in Slave mode or Multi-Master mode (more common). If MCU is acting as slave, then it can only listen to the GPS.
  If you want to send any configuration commands to GPS, then host needs to be in Master or Multi master mode.
- While Host (MCU) is in Master/Multi-Master mode, the following can be changed:

1) Clock rate can be switched to 100KHz (OSP command).
2) I²C address, (OSP command)
3) OSP/NMEA mode
4) GPS can be turn into a Slave mode by sending OSP Message ID 178, Sub ID 2 input command.

Change the GPS module from Multi master to Slave mode:

a. change from NMEA to OSP - "$PSRF100,0,115200,8,1,0*04\r\n".
b. Change to Slave mode with 400Kbps, send:
c. A0 A2 00 39 B2 02 00 F9 C5 68 03 FF 00 00 0B B8 09 0B 38 F9 00 01 03 FC 03 FC 00 04 00 3E 00 00 00 7C 00 00 00 00 00 00 00 00 00 00 00 00 00 01 C2 00 00 00 62 00 60 01 00 01 F4 00 01 0B 1D B0 B3 0D 0A
d. Read 128 Bytes at least from the GPS module, and then immediately without any delay send the next OSP message.
e. If you want to switch back from OSP to NMEA please use command
A0 A2 00 18 81 00 01 01 01 01 01 01 05 01 01 01 01 01 00 01 00 01 00 01
00 00 12 C0 01 66 B0 B3

GPS multi master	Host Salve
I²C address '0x60'	I²C address '0x62'
GPS slave	Host Master
I²C address '0x60'	I²C any address