OriginGPS
mini+mighty

MULTI SPIDER (ORG4572-R02 / R04)

GNSS RECEIVER MODULE

Datasheet

OriginGPS.com

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FIGURE INDEX

1. SCOPE

This document describes the features and specifications of Multi Spider ORG4572-R02/R04 GNSS receiver module.

2. DISCLAIMER

All trademarks are properties of their respective owners.
Performance characteristics listed in this document do not constitute a warranty or guarantee of product performance. OriginGPS assumes no liability or responsibility for any claims or damages arising out of the use of this document, or from the use of integrated circuits based on this document.
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OriginGPS reserves the right to make changes in its products, specifications and other information at any time without notice.
OriginGPS reserves the right to conduct, from time to time, and at its sole discretion, firmware upgrades. As long as those FW improvements have no material change on end customers, PCN may not be issued.
OriginGPS navigation products are not recommended to use in life saving or life sustaining applications.

3. SAFETY INFORMATION

Improper handling and use can cause permanent damage to the product.

4. ESD SENSITIVITY

This product is ESD sensitive device and must be handled with care.

5. CONTACT INFORMATION

Support - support@origingps.com or Online Form
Marketing and sales - marketing@origingps.com
Web – www.origingps.com

6. RELATED DOCUMENTATION

№	DOCUMENT NAME
1	Multi Spider – ORG4572 Evaluation Kit Datasheet
2	Spider and Hornet - NMEA Protocol Reference Manual
3	Spider and Hornet - OSP® Reference Manual
4	Spider and Hornet - OSP® GNSS Extensions Reference Manual
5	Spider and Hornet - Low Power Modes Application Note
6	SiRFLive FAQ

TABLE 1 – RELATED DOCUMENTATION

7. REVISION HISTORY

REVISION	DATE	CHANGE DESCRIPTION
1.0	October 18, 2016	First release
1.1	December 19,2016	Current and power consumption update
1.2	January 15, 2017	Height update
1.3	March 8, 2017	10Hz update, dimensions tolerance update, Architecture schematics update, Section 17.6 – smart sensors interface pads update. Section 17.7 – Flash memory update Section 17.7.2 – Aiding data storage support update Mechanical Specifications update
1.4	July 23, 2017	Section 17.4.1 – On_Off input - update Section 18.3 – Antenna switch - removal
1.5	October 10, 2017	MID 178 update
1.6	November 9, 2017	Default interface update – SPI V_{Backup} data update – in table 3 and table 4.
1.7	February 27, 2018	V_backup update Revision History – Section 21 update
1.8	April 23, 2018	Update Absolute Maximum Ratings table
1.9	May 29, 2018	Update Typical application circuit
2.0	Nov 27, 2018	Minor changes
2.1	Dec 30, 2018	Added 4572-R04
2.2	Jan 13, 2018	Added explanation about V_Battery in 4572-R04
2.3	Jan 21, 2018	Added appendix about V_Battery in 4572-R04
2.4	Feb 14, 2019	Update ON_OFF implementation Update Sensitivity
2.5	August 4, 2019	Updated Hibernate Current
2.6	Feb. 10, 2020	Update Mechanical Specifications
2.7	November 22, 2020	Update Ordering Information
2.8	February 28, 2022	Update SPI, Update ATP mode

TABLE 2 – REVISION HISTORY

8. GLOSSARY

A-GPS **A**ssisted **GPS**
ABP™ **A**lmanac **B**ased **P**osition
AC **A**lternating **C**urrent
ADC **A**nalog to **D**igital **C**onverter
AGC **A**utomatic **G**ain **C**ontrol
APM™ **A**daptive **P**ower **M**anagement
ATP™ **A**daptive **T**rickle **P**ower
BBRAM **B**attery **B**acked-up **RAM**
BE **B**roadcast **E**phemeris
BPF **B**and **P**ass **F**ilter
C/N_0 **C**arrier to **N**oise density ratio [dB-Hz]
CDM **C**harged **D**evice **M**odel
CE European Community conformity mark
CEP **C**ircular **E**rror **P**robability
CGEE™ **C**lient **G**enerated **E**xtended **E**phemeris
CMOS **C**omplementary **M**etal-**O**xide **S**emiconductor
CPU **C**entral **P**rocessing **U**nit
CTS **C**lear-**T**o-**S**end
CW **C**ontinuous **W**ave
DC **D**irect **C**urrent
DOP **D**ilution **O**f **P**recision
DR **D**ead **R**eckoning
DSP **D**igital **S**ignal **P**rocessor
ECHA **E**uropean **Ch**emical **A**gency
EE **E**xtended **E**phemeris
EGNOS **E**uropean **G**eostationary **N**avigation **O**verlay **S**ervice
EIA **E**lectronic **I**ndustries **A**lliance
EMC **E**lectro-**M**agnetic **C**ompatibility
EMI **E**lectro-**M**agnetic **I**nterference
ENIG **E**lectroless **N**ickel **I**mmersion **G**old
ESD **E**lectro-**S**tatic **D**ischarge
ESR **E**quivalent **S**eries **R**esistance
EU **E**uropean **U**nion
EVB **E**valuation **B**oard
EVK **E**valuation **K**it
FCC **F**ederal **C**ommunications **C**ommission
FSM **F**inite **S**tate **M**achine
GLONASS **GLO**bal **NA**vigation **S**atellite **S**ystem
GNSS **G**lobal **N**avigation **S**atellite **S**ystem
GPIO **G**eneral **P**urpose **I**nput or **O**utput
GPS **G**lobal **P**ositioning **S**ystem
HBM **H**uman **B**ody **M**odel
HDOP **H**orizontal **D**ilution **O**f **P**recision
I^2C **I**nter-**I**ntegrated **C**ircuit
I/O **I**nput or **O**utput
IC **I**ntegrated **C**ircuit
ICD **I**nterface **C**ontrol **D**ocument
IF **I**ntermediate **F**requency
ISO **I**nternational **O**rganization for **S**tandardization
JEDEC **J**oint **E**lectron **D**evice **E**ngineering **C**ouncil

LDO Low Dropout regulator
LGA Land Grid Array
LNA Low Noise Amplifier
LP Low Power
LS Least Squares
MID Message Identifier
MPM™ Micro Power Mode
MSAS Multi-functional Satellite Augmentation System
MSB Most Significant Bit
MSL Moisture Sensitivity Level
NFZ™ Noise-Free Zones System
NMEA National Marine Electronics Association
NVM Non-Volatile Memory
OSP® One Socket Protocol
PCB Printed Circuit Board
PLL Phase Lock Loop
PMU Power Management Unit
POR Power-On Reset
PPS Pulse Per Second
PRN Pseudo-Random Noise
PSRR Power Supply Rejection Ratio
PTF™ Push-To-Fix
QZSS Quasi-Zenith Satellite System
RAM Random Access Memory
REACH Registration, Evaluation, Authorisation and Restriction of Chemical substances
RF Radio Frequency
RHCP Right-Hand Circular Polarized
RMS Root Mean Square
RoHS Restriction of Hazardous Substances directive
ROM Read-Only Memory
RTC Real-Time Clock
RTS Ready-To-Send
SAW Surface Acoustic Wave
SBAS Satellite-Based Augmentation Systems
SGEE™ Server Generated Extended Ephemeris
SID Sub-Identifier
SIP System In Package
SMD Surface Mounted Device
SMPS Switched Mode Power Supply
SMT Surface-Mount Technology
SOC System On Chip
SPI Serial Peripheral Interface
SSB® SiRF Standard Binary
SV Satellite Vehicle
TCXO Temperature-Compensated Crystal Oscillator
TTFF Time To First Fix
TTL Transistor-Transistor Logic
UART Universal Asynchronous Receiver/Transmitter
VCCI Voluntary Control Council for Interference by information technology equipment
VEP Vertical Error Probability
VGA Variable-Gain Amplifier
WAAS Wide Area Augmentation System

9. ABOUT SPIDER FAMILY

OriginGPS GNSS receiver modules have been designed to address markets where size, weight, stand-alone operation, highest level of integration, power consumption and design flexibility - all are very important.
OriginGPS' Spider family breaks size barrier, offering the industry's smallest fully-integrated, highly-sensitive GPS / GNSS modules.
Spider family features OriginGPS' proprietary NFZ™ technology for high sensitivity and noise immunity even under marginal signal condition, commonly found in urban canyons, under dense foliage or when the receiver's position in space rapidly changes.
Spider family enables the shortest TTM (Time-To-Market) with minimal design risks.
Just connect an antenna and power supply on a 2-layer PCB.

10. ABOUT MULTI SPIDER MODULE

Multi Spider ORG4572 module is a complete SiP featuring miniature LGA SMT footprint designed to commit unique integration features for high volume cost sensitive applications.
Designed to support ultra-compact applications such as smart watches, wearable devices, trackers and digital cameras, ORG4572 module is a miniature multi-channel GPS/ GLONASS with SBAS, QZSS and other regional overlay systems receiver that continuously tracks all satellites in view, providing real-time positioning data in industry's standard NMEA format.
ORG4572 module offers superior sensitivity and outstanding performance, achieving rapid TTFF in less than one second, accuracy of approximately one meter, and tracking sensitivity of -167dBm.
Sized only 7mm x 7mm the ORG4572 GNSS module is pin and footprint compatible with OriginGPS' popular ORG4472 GPS and ORG4572-R01 GNSS modules.
Multi Spider ORG4572 module integrates LNA, SAW filter, TCXO, RTC crystal, RF shield and built in Flash memory, with market-leading SiRFstarV™ GNSS SoC.
Multi Spider ORG4572 module is capable to decode extremely weak satellite signals simultaneously from GPS and GLONASS thereby offering best-in-class positioning availability, unparalleled accuracy and extremely fast fixes under challenging signal conditions, such as in built-up urban areas, dense foliage or even indoor.
Internal GNSS SoC incorporating high-performance microprocessor and sophisticated GNSS firmware keeps positioning payload off the host allowing integration in embedded solutions even with low computing resources.
Innovative architecture can detect changes in context, temperature, and satellite signals to achieve a state of near continuous availability by maintaining and opportunistically updating its internal fine time, frequency, and ephemeris data while consuming mere microwatts of battery power.

11. ABOUT ORIGINGPS

OriginGPS is a world leading designer, manufacturer and supplier of miniature positioning modules, antenna modules and antenna solutions.
OriginGPS modules introduce unparalleled sensitivity and noise immunity by incorporating Noise Free Zone system (NFZ™) proprietary technology for faster position fix and navigation stability even under challenging satellite signal conditions.
Founded in 2006, OriginGPS is specializing in development of unique technologies that miniaturize RF modules, thereby addressing the market need for smaller wireless solutions.

12. DESCRIPTION

12.1. FEATURES

- Autonomous operation
- Pin compatible with ORG4472 GPS and ORG4572-R01 GNSS modules
- OriginGPS Noise Free Zone System (NFZ™) technology
- Fully integrating:
  Dual-stage GNSS LNAs, GNSS SAW Filter, TCXO, RTC Crystal, RF Shield, GNSS SoC, PMU
- Active or Passive antenna support
- GPS L1 1575.42 frequency, C/A code
- GLONASS L1 FDMA 1598-1606MHz frequency band, SP signal
- SBAS (WAAS, EGNOS, MSAS) and QZSS support
- Concurrent tracking of multiple constellations
- 52 channels
- Ultra-high Sensitivity down to -167dBm enabling Indoor Tracking
- TTFF of < 1s in 50% of trials under Hot Start conditions
- Low Power Consumption of < 15mW in ATP™ mode
- High Accuracy of < 1.5m in 50% of trials
- High update rate of 10Hz, 1Hz by default
- Built in 16M-Bit Flash memory
- Autonomous A-GNSS by Client Generated Extended Ephemeris (CGEE™) for non-networked devices
- Predictive A-GNSS by Server Generated Extended Ephemeris (SGEE™) for connected devices
- Ephemeris Push™ for storing and loading broadcast ephemeris
- Host controlled power saving mode
- Self-managed low power modes - ATP™, PTF™ and APM™.
- Almanac Based Positioning (ABP™)
- Multipath and cross-correlation mitigation
- Active Jammer Detector and Remover
- Smart Data Logging to external memory
- Fast Time Synchronization for rapid single satellite time solution
- ARM7® microprocessor system
- Selectable UART, SPI or I²C host interface
- NMEA protocol by default, switchable into One Socket Protocol (OSP®)
- Programmable baud rate and messages rate
- 1PPS output
- Smart sensors auxiliary I²C interface
- Antenna input matched 50Ω
- Single voltage supply
- Miniature LGA footprint of 7mm x 7mm
- Ultra-low height of 1.6 mm.
- Ultra-low weight of 0.2 gr.
- Surface Mount Device (SMD)
- Optimized for automatic assembly and reflow equipment
- Operating from -40°C to +85°C
- FCC, CE, VCCI certified
- RoHS II/REACH compliant

12.2. ARCHITECTURE

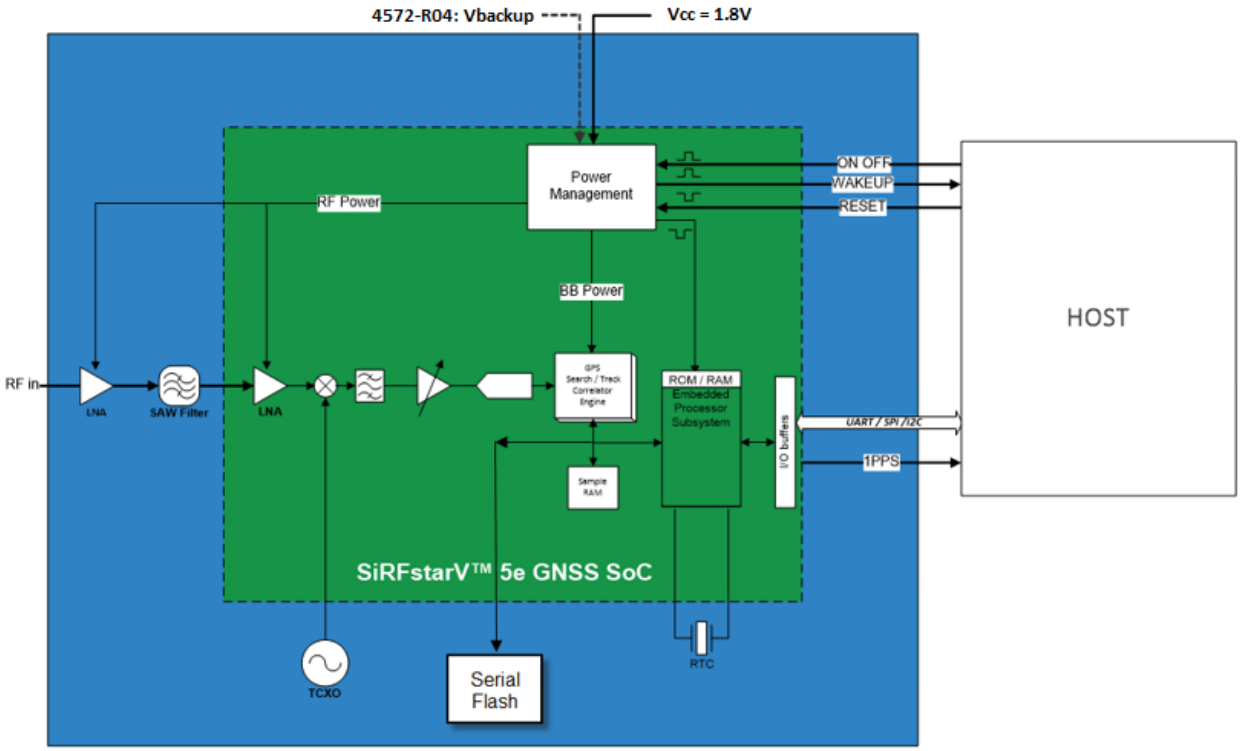


FIGURE 1 – ORG4572-R02 / R04 STANDARD ARCHITECTURE

GNSS SAW Filter

Band-Pass SAW filter eliminates out-of-band signals that may interfere to GNSS reception.
GNSS SAW filter is optimized for low insertion-loss in GNSS band and low return-loss outside it.

GNSS LNA

The integrated LNAs amplifies the GNSS signal to meet RF down converter input threshold.
Noise Figure optimized design was implemented to provide maximum sensitivity.

TCXO

Highly stable 26 MHz oscillator controls the down conversion process in RF block of the GNSS SoC.
Characteristics of this component are important factors for higher sensitivity, shorter TTFF and better navigation stability.

RTC crystal

Tuning fork quartz crystal with very tight specifications is necessary for maintaining Hot Start and Warm Start capabilities of the module.

RF Shield

RF enclosure avoids external interference from compromising sensitive circuitry inside the module.
RF shield also blocks module's internal high frequency emissions from being radiated.

SiRFstarV™ 5e B02 GNSS SoC

CSR 5e B02 is a 5-th generation SiRFstar™ product.
It is a hybrid positioning processor that combines GPS + GLONASS + Galileo / GPS + BEIDOU and SBAS data to provide a high-performance navigation solution.
SiRFstarV™ 5e B02 is a full SoC built on a low-power RF CMOS single-die, incorporating GNSS RF, GNSS baseband, integrated navigation solution software and ARM® processor.

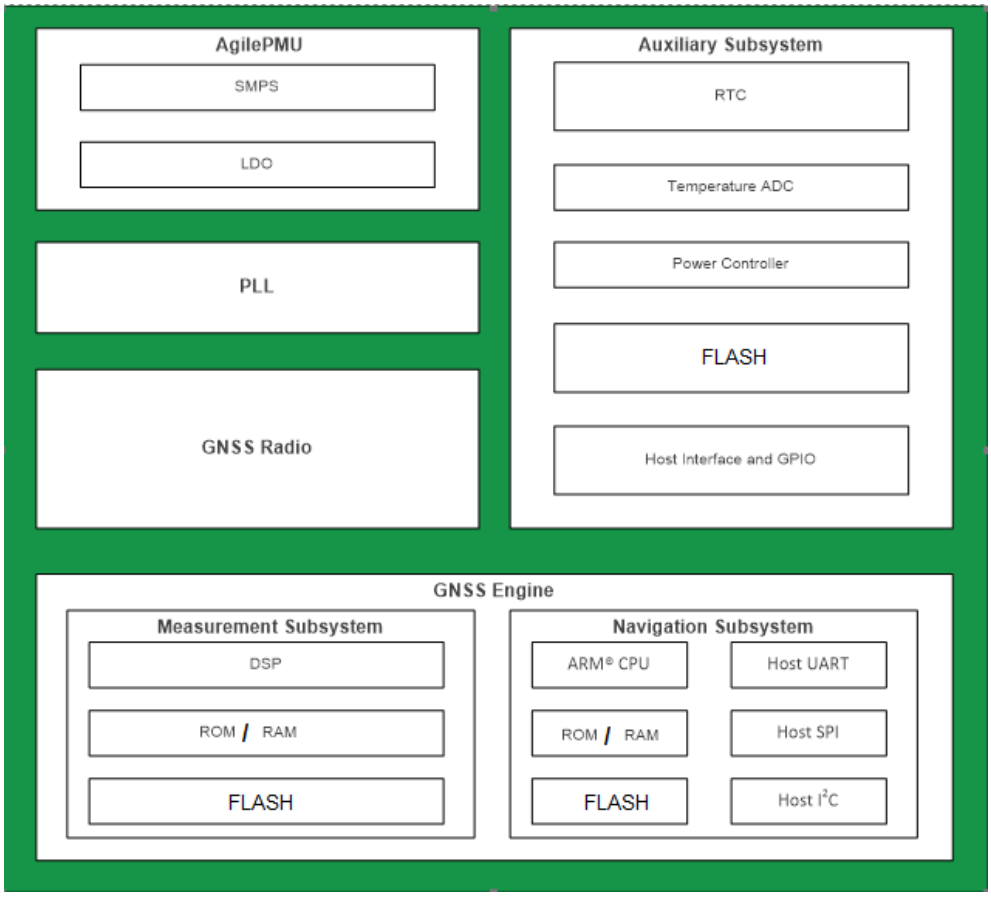


FIGURE 2 – SiRFstarV™ 5e B02 GNSS SoC BLOCK DIAGRAM

SiRFstarV™ 5e B02 SoC includes the following units:

- GNSS radio subsystem containing single input dual receive paths for concurrent GPS and GLONASS, harmonic-reject double balanced mixer, fractional-N synthesizer, integrated self-calibrating filters, IF VGA with AGC, high-sample rate ADCs with adaptive dynamic range.
- Measurement subsystem including DSP core for GNSS signals acquisition and tracking, interference scanner and detector, wideband and narrowband interference removers, multipath and cross-correlation detectors, dedicated DSP code ROM and DSP cache RAM.
- Measurement subsystem interfaces GNSS radio subsystem.
- Built in 16M-Bit Flash memory.

  Serial flash is required to store firmware, user configurations and system-aiding data.
- Navigation subsystem comprising ARM7® microprocessor system for position, velocity and time solution, program ROM, data RAM, cache and patch RAM, MEMS sensor driver, SPI flash driver, host interface UART, SPI and I²C drivers.
- Navigation subsystem interfaces measurement subsystem.
- Auxiliary subsystem containing RTC block and health monitor, temperature sensor for reference clock compensation, battery-backed SRAM for satellite data storage, voltage supervisor with POR, PLL controller, GPIO controller, 48-bit RTC timer and alarms, CPU watchdog monitor.
- Auxiliary subsystem interfaces navigation subsystem, PLL and PMU subsystems.
- PMU subsystem containing voltage regulators for RF and baseband domains.

13. ELECTRICAL SPECIFICATIONS

13.1. ABSOLUTE MAXIMUM RATINGS

Stresses exceeding Absolute Maximum Ratings may damage the device.

PARAMETER			SYMBOL	MIN	MAX	UNIT
Power Supply Voltage			V_{CC}		+4.50	V
Backup supply voltage **(Only for 4572-R04)**			V_{Backup}	+2.50	+4.50	V
Power Supply Current[1]			I_{CC}		150	mA
I/O Voltage			V_{IO}		+3.60	V
I/O Source/Sink Current			I_{IO}	-4	+4	mA
ESD Rating	I/O pads	HBM[2] method	$V_{IO(ESD)}$	-2000	+2000	V
		CDM[3] method		-400	+400	V
	RF input pad	HBM[2] method	$V_{RF(ESD)}$	-2000	+2000	V
RF Input Power	f_{IN} = 1560MHz÷1630MHz		P_{RF}		+10	dBm
	f_{IN} <1560MHz, >1630MHz				+30	dBm
Power Dissipation			P_D		350	mW
Operating Temperature			T_{AMB}	-40	+85	°C
Storage Temperature			T_{ST}	-55	+125	°C
Lead Temperature[4]			T_{LEAD}		+245	°C

TABLE 3 – ABSOLUTE MAXIMUM RATINGS

Notes:

1. Inrush current of up to 150mA for about 20µs duration.
2. Human Body Model (HBM) contact discharge per EIA/JEDEC JESD22-A114D.
3. Charged Device Model (CDM) contact discharge per JEDEC EIA/JESD22-C101.
4. Lead temperature at 1mm from case for 10s duration.

13.2. RECOMMENDED OPERATING CONDITIONS

Exposure to stresses above the Recommended Operating Conditions may affect device reliability.

PARAMETER	SYMBOL	MODE / PAD	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply voltage	V_{CC}	V_{CC}		+1.71	+1.80	+1.89	V
Backup supply voltage	V_{Backup}	V_{Backup}	**Only for 4572-R04**	+2.80	+3.60	+4.30	V
Power Supply Current[1]	I_{CC}	Acquisition	GPS		38		mA
			GPS+GLONASS		51		mA
		Tracking	GPS		39		mA
			GPS+GLONASS		49		mA
		ATP™ Tracking[2]			20		mA
		CPU only[3]			12		mA
		Standby[3]				0.1	mA
		PTF™[4]			0.4		mA
		Hibernate			29		µA
Input Voltage Low State	V_{IL}	GPIO		-0.30		+0.40	V
Input Voltage High State	V_{IH}			0.70·V_{CC}		+3.60	V
Output Voltage Low State	V_{OL}		I_{OL} = 2mA			+0.40	V
Output Voltage High State	V_{OH}		I_{OH} = -2mA	0.75·V_{CC}			V
Input Capacitance	C_{IN}				5		pF
Internal Pull-down Resistor	R_{PD}			0.11	1.00	2.80	MΩ
Input Leakage Current	$I_{IN(leak)}$		V_{IN} = 1.8V or 0V	-10		+10	µA
Output Leakage Current	$I_{OUT(leak)}$		V_{OUT} = 1.8V or 0V	-10		+10	µA
Input Impedance	Z_{IN}	RF Input	f_{IN} = 1575.5MHz		50		Ω
Input Return Loss	R_{LIN}			-7			dB
Input Power Range	P_{IN}		GPS or GLONASS	-167			dBm
Input Frequency Range	f_{IN}			1560		1620	MHz
Operating Temperature[5]	T_{AMB}			-40	+25	+85	°C
Storage Temperature	T_{ST}			-55	+25	+125	°C
Relative Humidity[6]	R_H		T_{AMB}	5		95	%

TABLE 4 – RECOMMENDED OPERATING CONDITIONS

Notes:

1. Typical values under conducted signal conditions of -130dBm and ambient temperature of +25°C.
2. ATP™ mode 200:1 (200ms on-time, 1s period), R02/R04 standard ordering option, GPS-only tracking.
3. Transitional states of ATP™ power saving mode.
4. PTF™ mode 30:30 (30s max. on-time – 18s typical, 30m period), R02/R04 standard ordering option, GPS-only tracking.
5. Longer TTFF is expected while operating below -30°C to -40°C.
6. Relative Humidity is within Operating Temperature range.

14. PERFORMANCE

14.1. ACQUISITION TIME

TTFF (Time To First Fix) – is the period of time from the module's power-up till position estimation.

14.1.1. HOT START

Hot Start results either from a software reset after a period of continuous navigation or a return from a short idle period that was preceded by a period of continuous navigation.
During Hot Start all critical data (position, velocity, time, and satellite ephemeris) is valid to the specified accuracy and available in RAM.

14.1.2. SIGNAL REACQUISITION

Reacquisition follows temporary blocking of GNSS signals.

Typical reacquisition scenario includes driving through tunnel.

14.1.3. AIDED START

Aided Start is a method of effectively reducing TTFF by providing valid satellite ephemeris data.

Aiding can be implemented using Ephemeris Push™, CGEE™ or SGEE™.

14.1.4. WARM START

Warm Start typically results from user-supplied position and time initialization data or continuous RTC operation with an accurate last known position available in RAM.
In this state position and time data are present and valid, but satellite ephemeris data validity has expired.

14.1.5. COLD START

Cold Start occurs when satellite ephemeris data, position and time data are unknown.

Typical Cold Start scenario includes first power application.

OPERATION[1]	MODE	VALUE	UNIT
Hot Start		< 1	s
Aided Start		< 10	s
Warm Start	GPS + GLONASS	< 26	s
	GPS	< 32	s
Cold Start	GPS + GLONASS	< 27	s
	GPS	< 35	s
Signal Reacquisition		< 1	s

TABLE 5 – ACQUISITION TIME

Notes:

1. EVK is 24-hrs. static under signal conditions of -130dBm and ambient temperature of +25°C.
2. Outage duration ≤ 30s.

14.2. SENSITIVITY

14.2.1. TRACKING

Tracking is an ability of receiver to maintain valid satellite ephemeris data.

During tracking receiver may stop output valid position solutions.

Tracking sensitivity defined as minimum GPS signal power required for tracking.

14.2.2. REACQUISITION

Reacquisition follows temporary blocking of GPS signals.

Reacquisition sensitivity defined as minimum GPS signal power required for reacquisition.

14.2.3. NAVIGATION

During navigation receiver consequently outputs valid position solutions.

Navigation sensitivity defined as minimum GPS signal power required for reliable navigation.

14.2.4. HOT START

Hot Start sensitivity defined as minimum GPS signal power required for valid position solution under Hot Start conditions.

14.2.5. AIDED START

Aided Start sensitivity defined as minimum GPS signal power required for valid position solution following aiding process.

14.2.6. COLD START

Cold Start sensitivity defined as minimum GPS signal power required for valid position solution under Cold Start conditions, sometimes referred as ephemeris decode threshold.

OPERATION[1]	MODE	VALUE	UNIT
Tracking	GPS	-167	dBm
	GLONASS	-165	dBm
Navigation	GPS	-164	dBm
	GLONASS	-164	dBm
Reacquisition[4]		-162	dBm
Hot Start[4]		-160	dBm
Aided Start[5]		-156	dBm
Cold Start	GPS	-148	dBm

TABLE 6 – SENSITIVITY

Notes:

1. EVK is static, ambient temperature is +25°C, RF signals are conducted.
2. R02/R04 - Dual-stage LNA standard ordering option.
3. Outage duration ≤ 30s.
4. Hibernate state duration ≤ 5m.
5. Aiding using Broadcast Ephemeris (Ephemeris Push™) or Extended Ephemeris (CGEE™ or SGEE™).

14.3. POWER CONSUMPTION

OPERATION[1]	MODE	VALUE	UNIT
Acquisition	GPS	68	mW
	GPS + GLONASS	92	mW
Tracking	GPS	70	mW
	GPS + GLONASS	88	mW
Low Power Tracking	ATP™ Tracking[3]	36	mW
	PTF™[4]	0.72	mW
	5m Hibernate: 10s tracking	2.3	mW
Hibernate		53	µW

TABLE 7 – POWER CONSUMPTION

Notes:

1. Typical values under conducted signal conditions of -130dBm and ambient temperature of +25°C.
2. R02/R04 - Dual-stage LNA standard ordering option.
3. ATP™ mode 200:1 (200ms on-time, 1s period), R02/R04 standard ordering option, GPS-only tracking.
4. PTF™ mode 30:30 (30s max. on-time – 18s typical, 30m period), R02/R04 standard ordering option, GPS-only tracking.

14.4. ACCURACY

PARAMETER		FORMAT	MODE	VALUE	UNIT
Position[1]	Horizontal	CEP (50%)	GPS + GLONASS	< 1.5	m
			GPS + SBAS	< 2.0	m
			GPS	< 2.5	m
		2dRMS (95%)	GPS + GLONASS	< 3.0	m
			GPS + SBAS	< 4.0	m
			GPS	< 5.0	m
	Vertical	VEP (50%)	GPS + GLONASS	< 2.5	m
			GPS + SBAS	< 3.5	m
			GPS	< 4.0	m
		2dRMS (95%)	GPS + GLONASS	< 5.0	m
			GPS + SBAS	< 6.5	m
			GPS	< 7.5	m
Velocity[2]	over ground	50% of samples		< 0.01	m/s
Heading	to north	50% of samples		< 0.01	°
Time[1]		RMS jitter	1 PPS	≤ 30	ns

TABLE 8 – ACCURACY

Notes:

1. Module is static under signal conditions of -130dBm, ambient temperature is +25°C.
2. EVK is 24-hrs. static, ambient temperature is +25°C.
3. Speed over ground ≤ 30m/s.

14.5. DYNAMIC CONSTRAINS

PARAMETER	Metric	Imperial
Velocity and Altitude[1]	515m/s and 18,288m	1,000knots and 60,000ft
Velocity	600m/s	1,166knots
Altitude	-500m to 24,000m	-1,640ft to 78,734ft
Acceleration	4g	
Jerk	$5m/s^3$	

TABLE 9 – DYNAMIC CONSTRAINS

Note:

1. Standard dynamic constrains according to regulatory limitations.

15. POWER MANAGEMENT

15.1. POWER STATES

15.1.1. FULL POWER ACQUISITION

ORG4572 module stays in Full Power Acquisition state until a reliable position solution is made. Switching to GPS-only mode turns off GLONASS RF block lowering power consumption.

15.1.2. FULL POWER TRACKING

Full Power Tracking state is entered after a reliable position solution is achieved.
During this state the processing is less intense compared to Full Power Acquisition, therefore power consumption is lower.
Full Power Tracking state with navigation update rate at 10 Hz / 5Hz consumes more power compared to default 1Hz navigation.

15.1.3. CPU ONLY

CPU Only is the transitional state of ATP™ power saving mode when the RF and DSP sections are partially powered off. This state is entered when the satellites measurements have been acquired, but navigation solution still needs to be computed.

15.1.4. STANDBY

Standby is the transitional state of ATP™ power saving mode when RF and DSP sections are completely powered off and baseband clock is stopped.

15.1.5. HIBERNATE

ORG4572 module boots into Hibernate state after power supply applied.
During this state RF, DSP and baseband sections are completely powered off leaving only RTC and Battery-Backed RAM running.
ORG4572 will perform Hot Start if stayed in Hibernate state less than 4 hours from last valid position solution.

15.2. BASIC POWER SAVING MODE

Basic power saving mode is elaborating host in straightforward way for controlling transfers between Full Power and Hibernate states.

Current profile of this mode has no hidden cycles of satellite data refresh.

Host may condition transfers by tracking duration, accuracy, satellites in-view or other parameters.

15.3. SELF MANAGED POWER SAVING MODES

Multi Spider module has several self-managed power saving modes tailored for different use cases.

These modes provide several levels of power saving with degradation level of position accuracy.

Initial operation in Full Power state is a prerequisite for accumulation of satellite data determining location, fine time and calibration of reference clocks.

15.3.1. ADAPTIVE TRICKLE POWER (ATP™)

ATP™ is best suited for applications that require navigation solutions at a fixed rate as well as low power consumption and an ability to track weak signals.
This power saving mode provides the most accurate position among self-managed modes.
In this mode module is intelligently cycled between Full Power state, CPU Only state consuming 15mA and Standby state consuming ≤ 0.1mA, therefore optimizing current profile for low power operation.
ATP™ period that equals navigation solution update can be 1 second to 3 seconds.
On-time including Full Power Tracking and CPU Only states can be 200ms to 900ms.

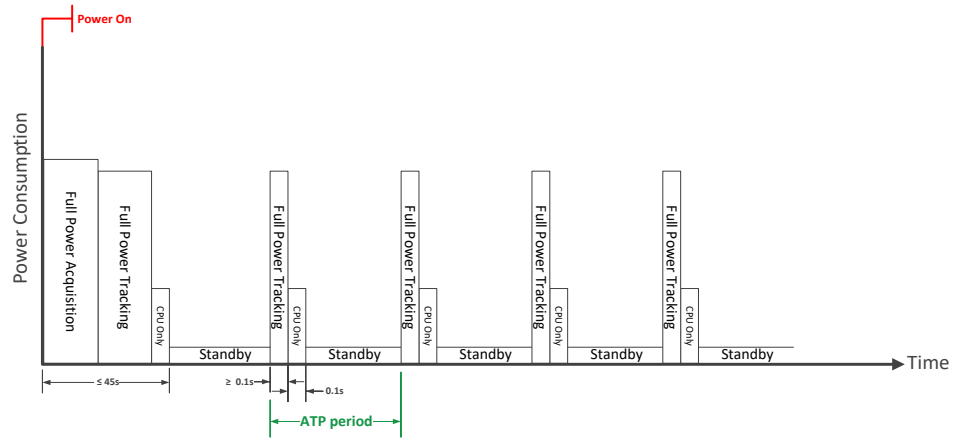


FIGURE 3 – ATP™ TIMING

15.3.2. PUSH TO FIX (PTF™)

PTF™ is best suited for applications that require infrequent navigation solutions.
In this mode ORG4572 module is mostly in Hibernate state, drawing ≤ 54µA of current, waking up for satellite data refresh in fixed periods of time.
PTF™ period can be anywhere between 10 seconds and 2 hours.
Host can initiate an instant position report by toggle the ON_OFF pad to wake up the module.
During fix trial module will stay in Full Power state until good position solution is estimated or pre-configured timeout for it has expired.

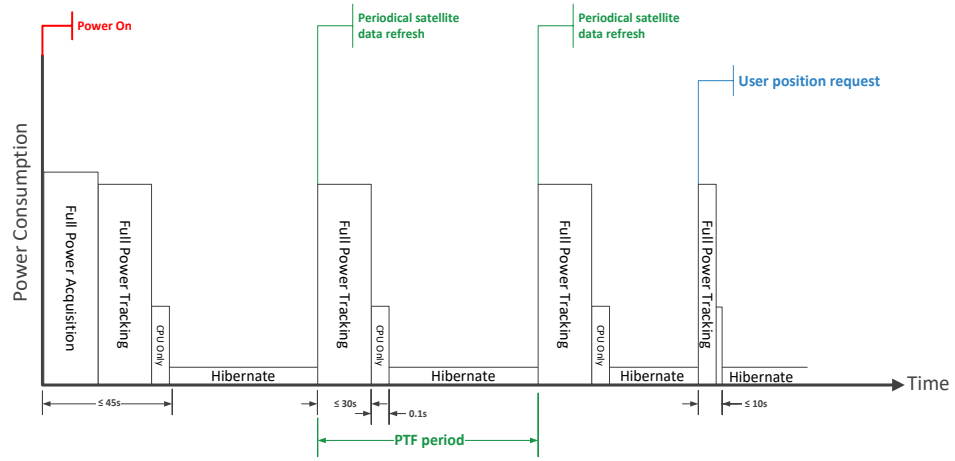


FIGURE 4 – PTF™ TIMING

15.3.3. ADVANCED POWER MANAGEMENT (APM™)

APM™ mode is designed for Aided-GPS wireless applications.
APM™ allows power savings while ensuring that the **Q**uality **o**f the **S**olution (QoS) in maintained when signals level drop.
In APM™ mode the module is intelligently cycled between Full Power and Hibernate states.
In addition to setting the position report interval, a QoS specification is available that sets allowable error estimates and selects priorities between position report interval and more power saving.
User may select between Duty Cycle Priority for more power saving and Time Between Fixes (TBF) priority with defined or undefined maximum horizontal error.
TBF range is from 10s to 180s between fixes, Power Duty Cycle range is between 5% to 100%.
Maximum position error is configurable between 1 to 160m.
The number of APM™ fixes is configurable up to 255 or set to continuous.

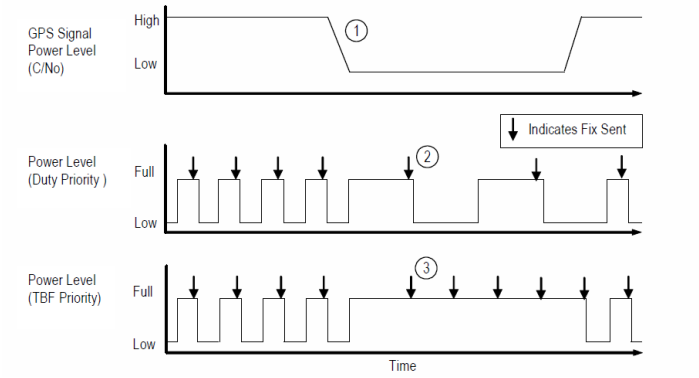


FIGURE 5 – APM™ TIMING

Notes:
1. GPS signal level drops (e.g. user walks indoor).
2. Lower signal results in longer ON time. To maintain Duty Cycle Priority, OFF time is increased.
3. Lower signal means missed fix. To maintain future TBFs module goes Full Power state until signal levels improve.

15.4. SMARTGNSS™ POWER MODES

In addition to the mentioned above power modes, ORG4572-R02/R04 introduces two new power saving modes, SiRFSmartGNSS I and SiRFSmartGNSS II, for continuous tracking and position reporting similar to full power. SiRFSmartGNSS modes are power saving alternatives for both GPS and GNSS operation while maintaining complete functionality of the device similar to full power.

ORG4572-R02/R04 will always default to full power during the initial acquisition of the first fix, and will continue tracking in SiRFSmartGNSS if enabled. Therefore all first fix metrics for SiRFSmartGNSS are equivalent to full power performance. Power consumption will vary based on signal strength.

15.4.1. SiRFSmartGNSS™ I

SiRFSmartGNSS I autonomously manage the GPS or GNSS system usage based on satellite signal strength to save power. The adaptive mechanism will use fewer system resources during strong signal conditions and use more resources during weak signal conditions in order to maintain superior navigation performance. Full constellation tracking is maintained while in this mode. The criteria to enter and remain in SiRFSmartGNSS I is a valid position fix with 6 or more satellites above 24 dB-Hz, otherwise the receiver switches to full power.

15.4.2. SiRFSmartGNSS™ II

SiRFSmartGNSS II includes the benefits of SiRFSmartGNSS I and achieves further power reduction by minimizing the usage of the secondary GNSS constellation. The adaptive mechanism will adjust constellation usage based on GPS signal conditions to maintain good performance while minimizing power. As an example, in the case of GPS + GLONASS mode of operation, the GLONASS satellite usage will be minimized during strong GPS satellite conditions. SiRFSmartGNSS II is only applicable for multi-constellation operation.
The criteria to enter and remain in SiRFSmartGNSS II is a valid position fix with 4 or more satellites above 24 dB-Hz, otherwise the receiver switches to full power.

15.4.3. SiRFAware™

SiRFAware™ is a very low-power maintenance mode. The objective of SiRFAware is to remain below a stated average current level while maintaining a low level of uncertainty in time, frequency, position and ephemeris state.
SiRFAware™ operates by capturing a buffer of GPS samples at infrequent intervals and analyzing the data to update its time, frequency and position estimates. For satellites needing updated ephemeris data, a data collection is scheduled when strong signals are detected. During the data collection phase, time and frequency calibration operations are also carried out.

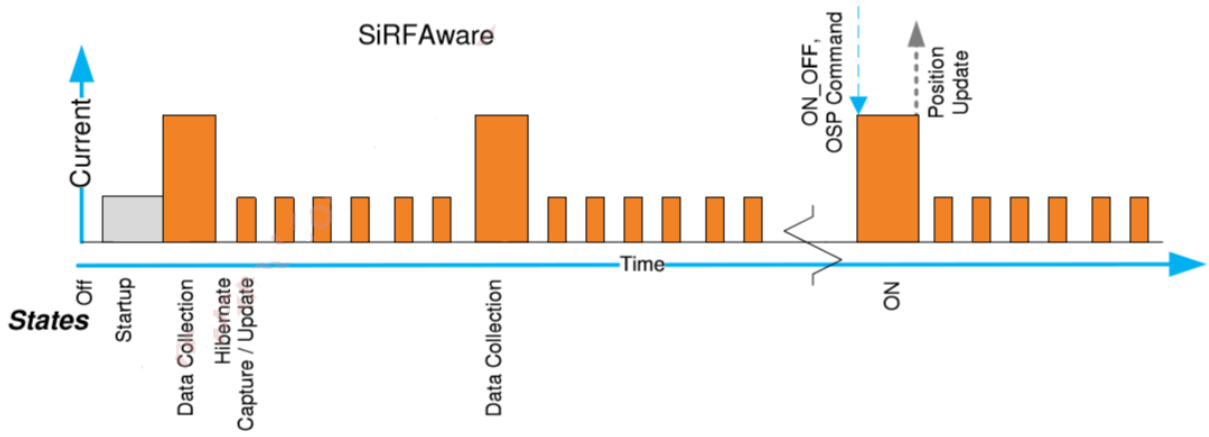


Figure 6 - SiRFAware™ Current Profile

Typical Capture/Update frequency varies: about once every ten minutes for 9 seconds. Data collection in SiRFAware is managed to limit power consumption. When data collection is required, it is timed to collect just the required data. Data collection is twice an hour at ~18 seconds each.
SiRFAware allows the user to make the request at any time. The criterion to enter and remain in SiRFAware cycling is a valid Kalman-Filter position fix. If the receiver cannot transition to its cycling mode it will sleep for 10 minutes and try again. If signals are strong enough to get the initial ephemeris to make a valid navigation solution, the receiver will stay awake to collect the data and start a successful SiRFAware cycle.

16. EXTENDED FEATURES

16.1. ALMANAC BASED POSITIONING (ABP™)

With ABP™ mode enabled, the user can get shorter Cold Start TTFF as tradeoff with position accuracy.

When no sufficient ephemeris data is available to calculate an accurate solution, a coarse solution will be provided where the position is calculated based on one or more of the GPS satellites, having their states derived from the almanac data.

Data source for ABP™ may be either stored factory almanac, broadcasted or pushed almanac.

16.2. ACTIVE JAMMER DETECTOR AND REMOVER

Jamming Detector is embedded DSP software block that detects interference signals in GPS L1 and GLONASS L1 band.

Jamming Remover is additional DPS software block that sort-out Jamming Detector output mitigating up to 8 interference signals of Continuous Wave (CW) type up to 80dB-Hz each.

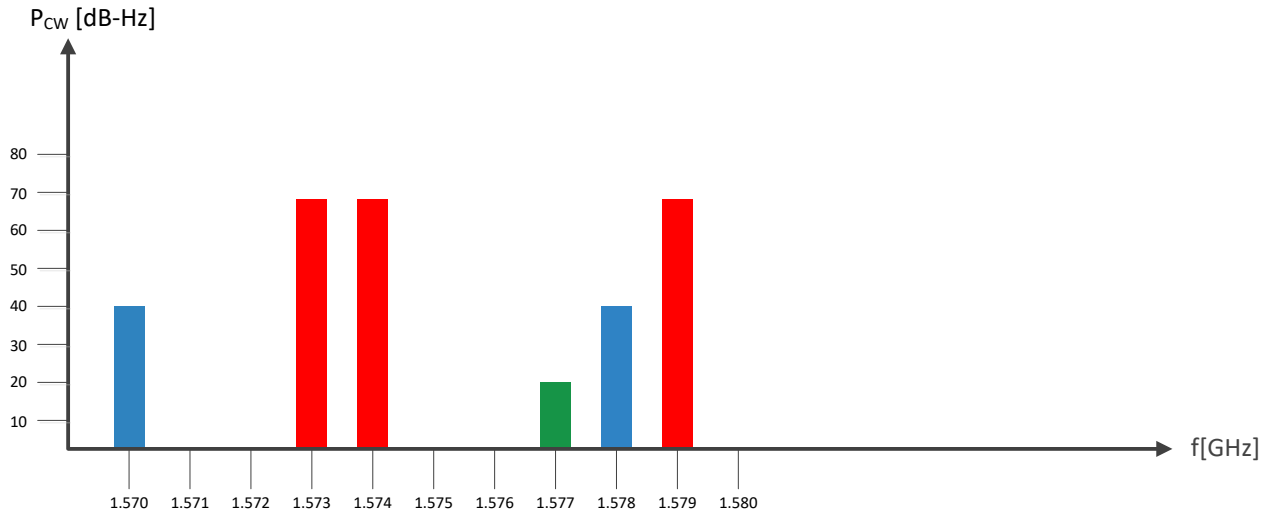


FIGURE 7 – ACTIVE JAMMER DETECTOR FREQUENCY PLOT

16.3. CLIENT GENERATED EXTENDED EPHEMERIS (CGEE™)

CGEE™ feature allows shorter TTFFs by providing predicted (synthetic) ephemeris files created within a non-networked host system from previously received satellite ephemeris data.

The prediction process requires good receipt of broadcast ephemeris data for all satellites.

EE files created this way are good for up to 3 days and then expire.

CGEE™ feature requires avoidance of power supply removal.

CGEE™ data files are stored and managed by host.

16.4. SERVER GENERATED EXTENDED EPHEMERIS (SGEE™)

SGEE™ enables shorter TTFFs by fetching **E**xtended **E**phemeris (EE) file downloaded from web server.

Host is initiating periodic network sessions of EE file downloads, storage and provision to module.

There is one-time charge for set-up, access to OriginGPS EE distribution server and end-end testing for re-distribution purposes, or there is a per-unit charge for each module within direct SGEE™ deployment.

GPS EE files are provided with look-ahead of 1, 3, 7, 14 or 31 days.
GLONASS EE files are provided with look-ahead of 1, 3, 7 or 14 days.

17. INTERFACE

17.1. PAD ASSIGNMENT

Please notice: There is a change in the numbering of pins in ORG4572-R02/R04, compared to ORG4572-R01. All GPIO are disabled by default.

PAD	NAME	FUNCTION			DIRECTION
1	GND	System Ground			Power
2	RF_IN	Antenna Signal Input			Analog Input
3	GND	System Ground			Power
4	WAKEUP	Power Status			Output
5	GPIO2	GPIO			Bi-directional
6	$\overline{\text{RESET}}$	Asynchronous Reset			Input
7	$\overline{\text{CTS}}$	Interface Select 1	UART Clear To Send	SPI Clock	Bi-directional
8	$\overline{\text{RTS}}$	Interface Select 2	UART Ready To Send	SPI Chip Select	Bi-directional
9	RX	UART Receive	SPI Data In	I^2C Data	Bi-directional
10	GPIO8	GPIO			Bi-directional
11	ON_OFF	Power State Control			Input
12	1PPS	UTC Time Mark			Output
13	TX	UART Transmit	SPI Data Out	I^2C Clock	Bi-directional
14	V_{CC}	System Power			Power
15	V_backup / NC	Battery input for 4572-R04 / Not connected for 4572-R02			Power / NC
16	NC	Not Connected			
17	GND	System Ground			Power
18	GPIO B	GPIO			Bi-directional
19	GPIO C	GPIO			Bi-directional
20	NC	Not Connected			

TABLE 10 – PIN-OUT

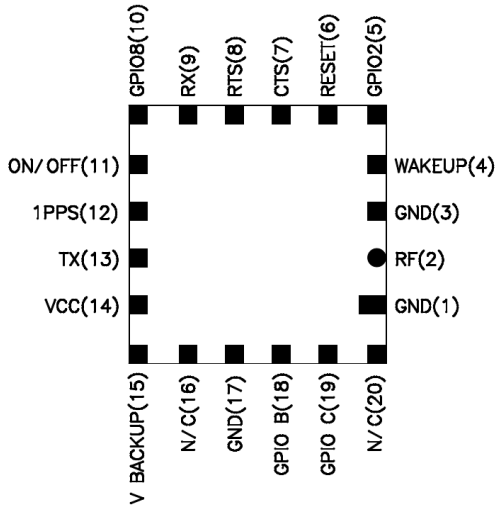


FIGURE 8 – PAD ASSIGNMENT TOP VIEW

17.2. POWER SUPPLY

It is recommended to keep the power supply on all the time in order to maintain RTC block active and keep satellite data in RAM for fastest possible TTFF.
When V_{CC} is removed settings are reset to factory default and the receiver performs Cold Start on next power up.

17.2.1. V_{CC} = 1.8V

V_{CC} is 1.8V ±5% DC and must be provided from regulated power supply.
Inrush current is up to 150mA for about 20µs duration, V_{CC} can be dropped down to 1.66V.
Typical I_{CC} during acquisition is 51mA on R02/R04 standard ordering option.
Lower acquisition current is possible disabling GLONASS radio path by software command.
During tracking the processing is less intense compared to acquisition, therefore power consumption is lower.
Maximum I_{CC} current in Hibernate state is 30µA, while all I/O lines externally held in Hi-Z state.
Output capacitors are critical when powering ORG4572 from switch-mode power supply.
Filtering is important to manage high alternating current flows on the power input connection.
An additional LC filter on ORG4572 power input may be needed to reduce system noise.
The high rate of ORG4572 input current change requires low ESR bypass capacitors.
Additional higher ESR output capacitors can provide input stability damping.
The ESR and size of the output capacitors directly define the output ripple voltage with a given inductor size. Large low ESR output capacitors are beneficial for low noise.
Voltage ripple below 50mV_{PP} allowed for frequencies between 100KHz to 1MHz.
Voltage ripple below 15mV_{PP} allowed for frequencies above 1MHz.
Higher voltage ripple may compromise ORG4572 performance.

17.2.2. V_BACKUP

Only for 4572-R04
In order to maintain configuration settings after a power cycle, the backup power is necessary.
V_backup is also necessary to save information such as SGEE and almanac on flash, without the need to upload this data after a power cycle. Storing this information will provide faster TTFF.
Important: For regular operation of the module, V_backup input is a must!
In case you don't use a battery, you must connect the V_backup to the VCC.
In this case the VCC must be a typical value of 3.3V instead of 1.8V.
Vio will stay 1.8V TTL.

17.2.3. GROUND

Ground pads must be connected to host PCB Ground with shortest possible traces or vias.

17.3. RF INPUT

RF input impedance is 50Ω, DC blocked up to ±25V.
Multi Spider ORG4572-R02/R04 supports active or passive antennas.

17.3.1. PASSIVE ANTENNA

R02/R04 standard ordering option incorporating dual-stage LNA is highly recommended for design with passive antenna, due to it's ultimate sensitivity.
Short trace of 50Ω controlled impedance should conduct GNSS signal from antenna to RF_IN pad.
In design with passive antenna attention should be paid on antenna layout.

17.3.2. ACTIVE ANTENNA

Active antenna net gain including conduction losses should not exceed +25dB.
DC bias voltage for active antenna can be externally applied on RF_IN trace through bias-T.

DC bias voltage can be controlled by WAKEUP output through MOSFET or load switch.
In design with external LNA power enable can be controlled by ORG4572 WAKEUP output that by following module's power states assists reducing overall system current consumption.

17.4. CONTROL INTERFACE

17.4.1. ON_OFF

ON_OFF input is used to switch ORG4572-R02/R04 between different power states:

- High-level input initiates system transitions from Hibernate to Full Power.
  The module will remain in full power state as long as ON_OFF input is high.
- Low-level input initiates transition from full power to Hibernate.
  The module will remain in Hibernate state as long as ON_OFF input is low.
- While in PTF™ mode, an ON_OFF pulse will initiate one PTF™ request. The module will wait for a fix, update required satellites data and go back to Hibernate mode.

17.4.2. WAKEUP

WAKEUP output from ORG4572-R02/R04 is used to indicate power state.
A low logic level indicates that the module is in one of its low-power states - Hibernate or Standby. A high logic level indicates that the module is in Full Power state.
In addition WAKEUP output can be used to control auxiliary devices.
Wakeup output is LVCMOS 1.8V compatible.
Do not connect if not in use.

17.4.3. $\overline{\text{RESET}}$

Power-on-Reset (POR) sequence is generated internally.
In addition, external reset is available through $\overline{\text{RESET}}$ pad.
Resetting module clears the state machine of self-managed power saving modes to default.
$\overline{\text{RESET}}$ signal should be applied for at least 1µs.
$\overline{\text{RESET}}$ input is active low and has internal pull-up resistor of 1MΩ.
Do not drive this input high.
Do not connect if not in use.

17.4.4. 1PPS

Pulse-Per-Second (PPS) output provides a pulse signal for timing purposes.
PPS output starts when 3D position solution has been obtained using 5 or more GNSS satellites.
PPS output stops when 3D position solution is lost.
Pulse length (high state) is 200ms with rising edge is less than 30ns synchronized to UTC epoch.
The correspondent UTC time message is generated and put into output FIFO 300ms after the PPS signal. The exact time between PPS and UTC time message delivery depends on message rate, message queue and communication baud rate.
1PPS output is LVCMOS 1.8V compatible.
Do not connect if not in use.

17.4.5. BOOT MODE

SiRFstarV always starts up in Boot mode when it comes out of a reset or at initial power up. It then performs three tests. If all three tests pass, SiRFstarV switches to Operational mode. If any of the tests fail, SiRFstarV remains in Boot mode and waits for input, usually from SiRFLive, SiRFFlashcl or similar tools.
The Order of the tests performed is:

1. Test of serial flash. If flash is corrupted, go to Boot mode.
2. Read BOOTMODE pin. If pulled high, go to Boot mode.
3. Test the data in serial flash against a stored CRC32. If the test fails, go to Boot mode.

17.4.6. Second I2C port

The second I2C port is used to connect MEMS sensors in a master-slave mode.
This is additional I2C port. The main I2C port is working in multi-master mode.

17.5. DATA INTERFACE

ORG4572-R02/R04 module has 3 types of interface ports to connect to host - UART, SPI or I²C – all multiplexed on a shared set of pads. At system reset host port interface lines are disabled, so no conflict occurs.
Logic values on $\overline{CTS}$ and $\overline{RTS}$ are read by the module during startup and define host port type. External resistor of 10kΩ is recommended. Pull-up resistor is referenced to 1.8V.

PORT TYPE	$\overline{CTS}$	$\overline{RTS}$
UART	External pull-up	Internal pull-up
SPI (default)	Internal pull-down	Internal pull-up
I²C	Internal pull-down	External pull-down

TABLE 11 – HOST INTERFACE SELECT

17.5.1. UART

Multi Spider ORG4572-R02/R04 has a standard UART port:

- TX used for GNSS data reports. Output logic high voltage level is LVCMOS 1.8V compatible.
- RX used for receiver control. Input logic high voltage level is 1.45V tolerable up to 3.6V.
- UART flow control using $\overline{CTS}$ and $\overline{RTS}$ lines is disabled by default.
  Can be turned on by sending OSP® Message ID 178, Sub ID 70 input command.

17.5.2. SPI

SPI host interface features are:

- Slave SPI Mode 1, supports clock up to 6.8MHz.
- RX and TX have independent 2-byte idle patterns of '0xA7 0xB4'.
- TX and RX each have independent 1024 byte FIFO buffers.
- TX FIFO is disabled when empty and transmits its idle pattern until re-enabled.
- RX FIFO detects a software specified number of idle pattern repeats and then disables FIFO input until the idle pattern is broken.
- FIFO buffers can generate an interrupt at any fill level.
- SPI detects synchronization errors and can be reset by software.
- Output is LVCMOS 1.8V compatible. Inputs are tolerable up to 3.6V.
- If idle bytes are still applied for more than one second when expected to receive data, please toggle ON_OFF pin to wake up the module.

17.5.3. I²C

I²C host interface features are:

- I²C Multi-Master Mode - module initiates clock and data, operating speed 400kbps.
- I²C address '0x60' for RX and '0x62' for TX.
- Individual transmit and receive FIFO length of 64 bytes.
- I²C host interface mode can be switched slave (Multi-master default), clock rate can be switched 100KHz (default 400KHz), address can be changed (default 0x62 for TX FIFO and 0x60 for RX FIFO) by sending OSP® Message ID 178, Sub ID 70 input command.
- SCL and SDA are pseudo open-drain lines, therefore require external pull-up resistors of 2.2kΩ to 1.8V, or 3.3kΩ to 3.3V.

17.6. SMART SENSORS INTERFACE

MEMS sensors connected to an auxiliary I²C bus provide support for contextual awareness.
I²C bus comprises of 2 pads – GPIOB and GPIOC, both are pseudo open-drain therefore requiring external pull-up resistors.

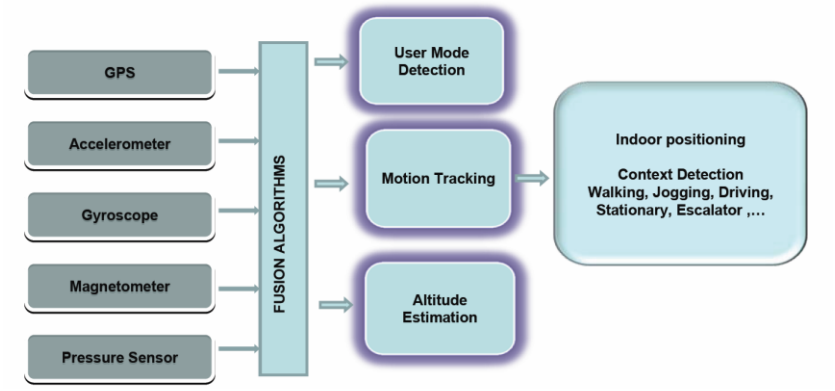


FIGURE 9 – SMART SENSORS INTERFACE

ORG4572 acts as I²C Master and sensor devices function in Slave mode at speed of 400kbps.
This provides a very low latency data pipe for the critical sensor data so that it can be used in the Navigation Library and Kalman filter to enhance navigation performance.
MEMS algorithms perform a sensor data fusion with GNSS signal measurements.
GNSS measurements can be used to calibrate MEMS sensors during periods of satellite navigation.
MEMS sensors can augment GNSS measurements, making those more accurate under degraded satellite signal conditions and challenging dynamics.
MEMS data can be output to other subsystems in the platform over host serial interface.

17.7. FLASH MEMORY INTERFACE

ORG4572-R02/R04 includes internal 16MBit flash memory. The flash memory is used for system aiding data, smart data logger, firmware update.

17.7.1. DATA LOGGER SUPPORT

ORG4572 can log data waypoints to SPI flash memory autonomously or under host control.
Features of data logger include:

- Ability to log based on time interval and/or when distance or speed thresholds are exceeded.
- Control over logging continuously or until available memory is full.
- Control over which data is logged, including time, position, altitude, speed and accuracy.
- Access to status information on how much memory remains.
- Commands to clear memory and download data.

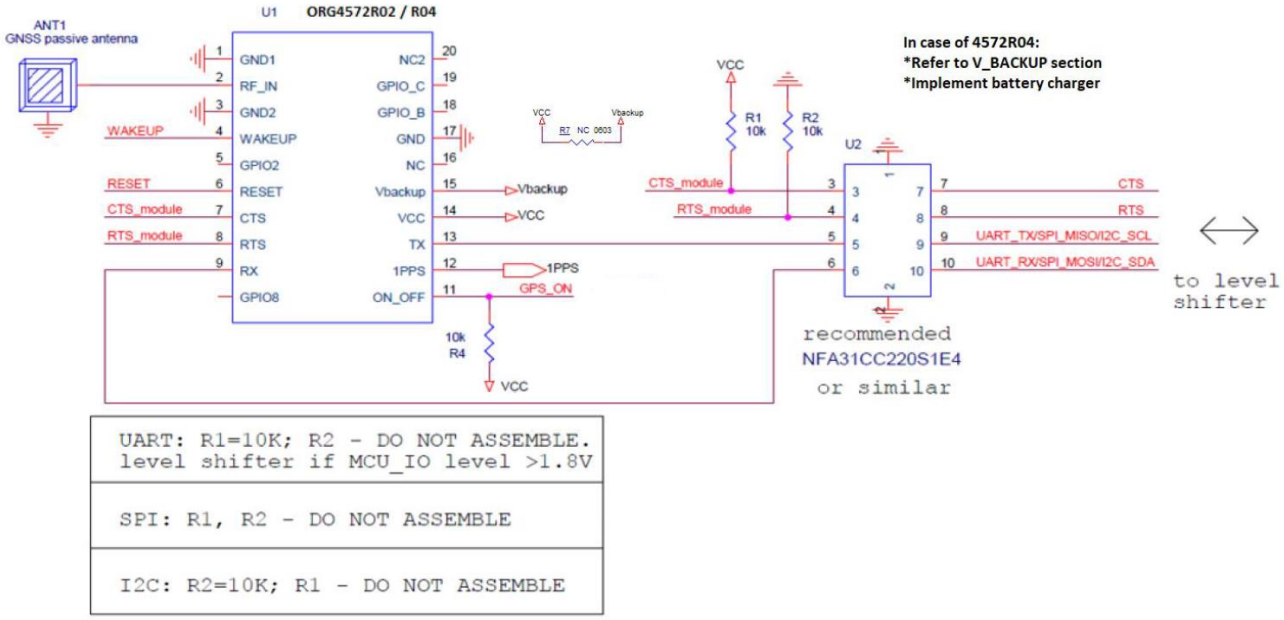
17.7.2. AIDING DATA STORAGE SUPPORT

ORG4572 stores CGEE™ and SGEE™ aiding data to SPI flash memory:

- ORG4572-R02/R04 contains 16Mbit flash memory, which supports up to 31 days of SGEE™ for GPS and 14 days for GLONASS.

18. TYPICAL APPLICATION CIRCUIT

18.1. PASSIVE ANTENNA



UART: R1=10K; R2 - DO NOT ASSEMBLE. level shifter if MCU_IO level >1.8V
SPI: R1, R2 - DO NOT ASSEMBLE
I2C: R2=10K; R1 - DO NOT ASSEMBLE

FIGURE 10 – PASSIVE ANTENNA REFERENCE SCHEMATICS

18.2. ACTIVE ANTENNA

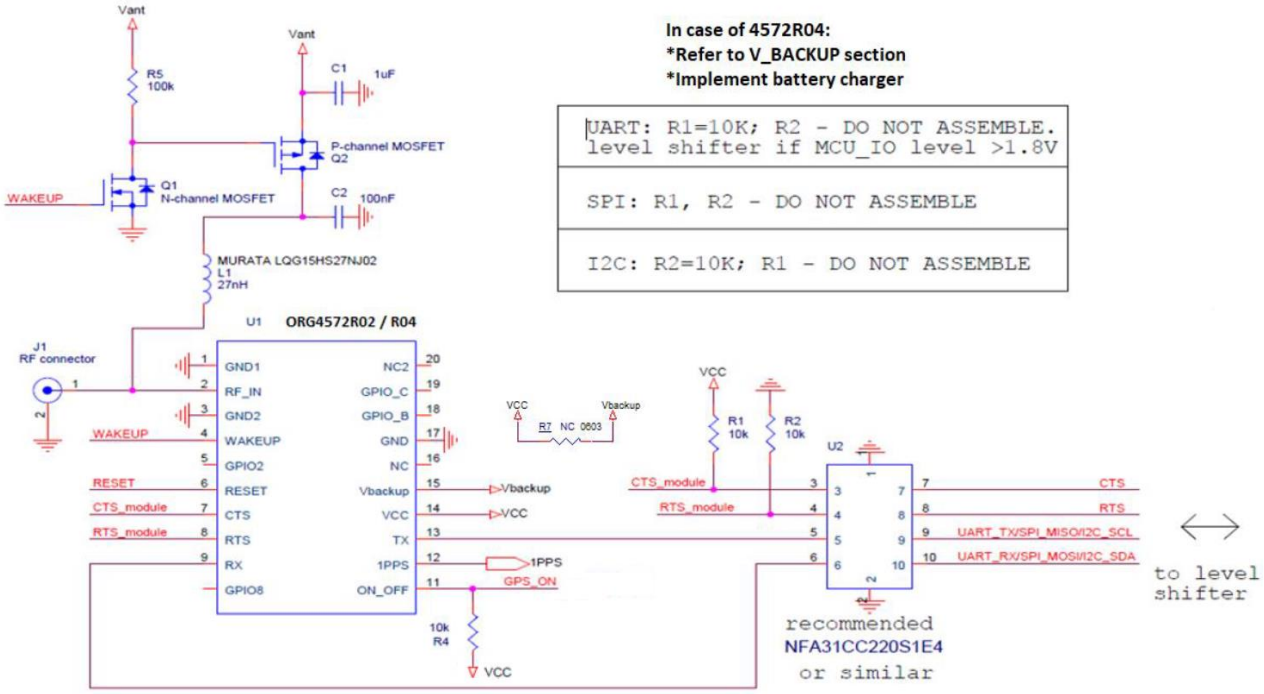


FIGURE 11 – ACTIVE ANTENNA REFERENCE SCHEMATICS

19. RECOMMENDED PCB LAYOUT

19.1. FOOTPRINT

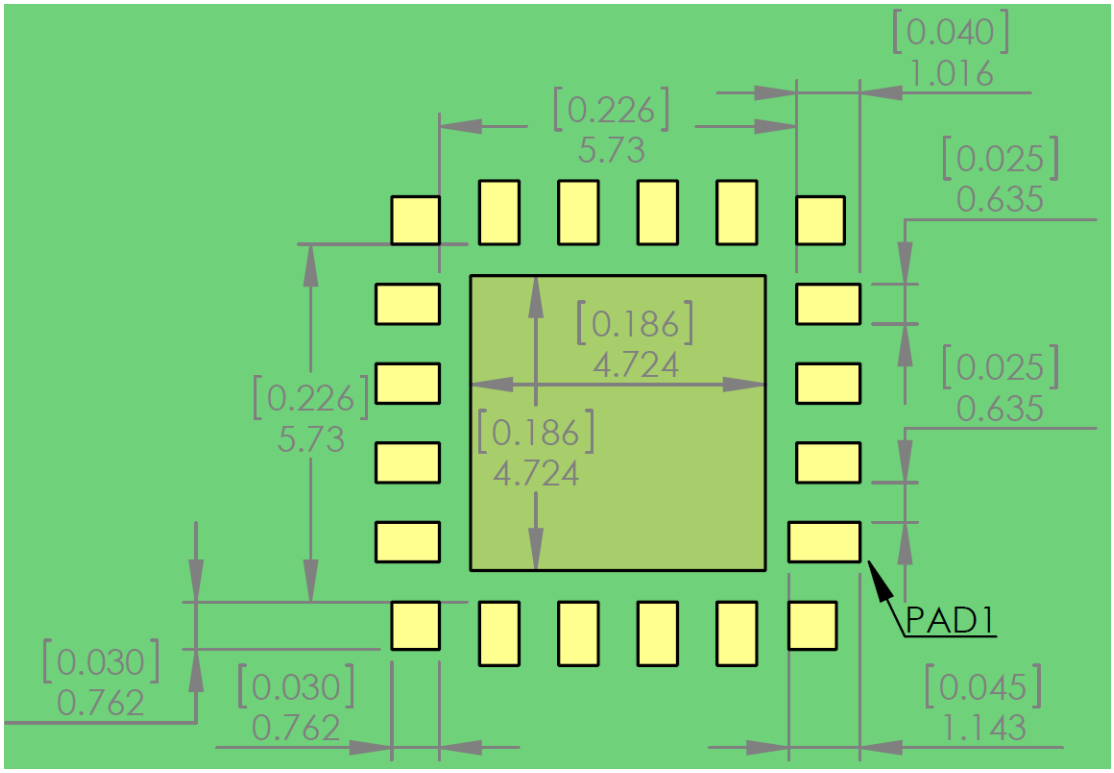


FIGURE 12 – FOOTPRINT

Ground paddle at the middle should be connected to main Ground plane by multiple vias.

Ground paddle at the middle must be solder masked.

Silk print of module's outline is highly recommended for SMT visual inspection.

TOP VIEW

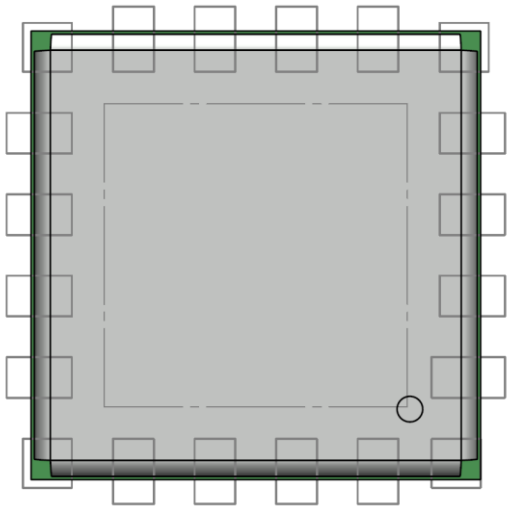


FIGURE 13 – MODULE HOSTED ON FOOTPRINT

19.2. HOST PCB

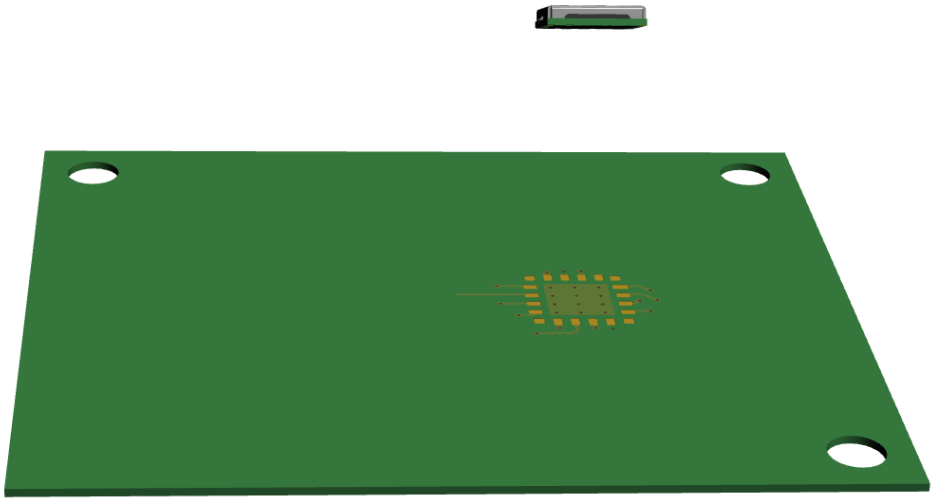


FIGURE 14 – HOST PCB

19.3. RF TRACE

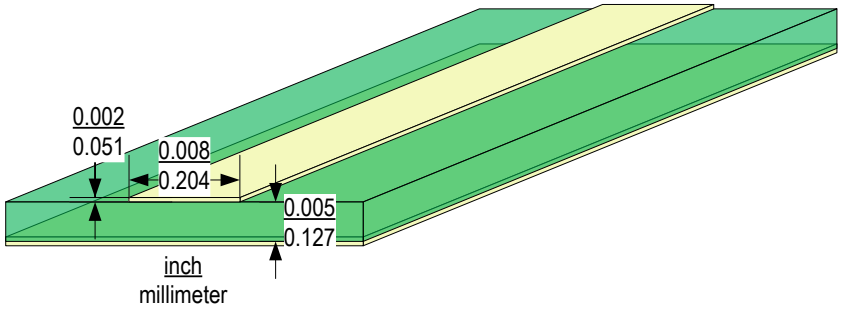


FIGURE 15 – TYPICAL MICROSTRIP PCB TRACE ON FR-4 SUBSTRATE

19.4. PCB STACK-UP

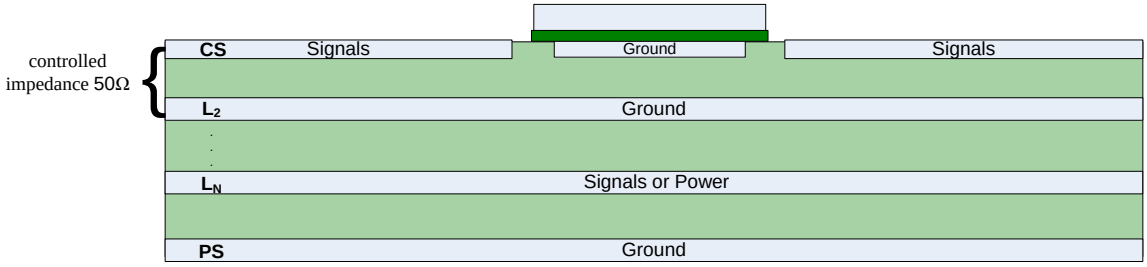


FIGURE 16 – TYPICAL PCB STACK-UP

19.5. PCB LAYOUT RESTRICTIONS

Switching and high-speed components, traces and vias must be kept away from ORG4572 module.
Signal traces to/from module should have minimum length.
Recommended minimal distance from adjacent active components is 3mm.
Ground pads must be connected to host PCB Ground with shortest possible traces or vias.
In case of tight integration constrain or co-location with adjacent high speed components like CPU or memory, high frequency components like transmitters, clock resonators or oscillators, LCD panels or CMOS image sensors, contact OriginGPS for application specific recommendations.

20. DESIGN CONSIDERATIONS

20.1. ANTENNA

Antennas for GPS and GLONASS have a wider bandwidth than pure GPS antennas.
Some wideband antennas may not have a good axial ratio to block reflections of RHCP GPS and GLONASS signals. These antennas have lower rejection of multipath reflections and tend to degrade the overall performance of the receiver.

20.1.1. PASSIVE ANTENNA

Design with passive antenna requires RF layout skills and can be challenging.

20.1.2. ACTIVE ANTENNA

While designing with active antenna consider using WAKEUP output to control auxiliary DC bias.

20.2. RF

Multi Spider ORG4572-R02/R04 operates with received signal levels down to -167dBm and can be affected by high absolute levels of RF signals, moderate levels of RF interference near the GNSS bands and by low-levels of RF noise in the GNSS band.
RF interference from nearby electronic circuits or radio transmitters can contain enough energy to desensitize ORG4572. These systems may also produce levels of energy outside of GNSS band, high enough to leak through RF filters and degrade the operation of the radios in ORG4572.
This issue becomes more critical in small products, where there are industrial design constraints.
In that environment, transmitters for Wi-Fi, Bluetooth, RFID, cellular and other radios may have antennas physically close to the GNSS receiver antenna.
To prevent degraded performance of ORG4572-R02/R04, OriginGPS recommends performing EMI/jamming susceptibility tests for radiated and conducted noise on prototypes and assessing risks of other factors.

Contact OriginGPS for application specific recommendations and design review services.

21. OPERATION

When power is first applied, module goes into a Reset state.
If $\overline{\text{RESET}}$ input is low, the module will remain in Reset state.
If $\overline{\text{RESET}}$ input is not low – the module will transit to Hibernate state.
While in Hibernate state, module awaits a high input on ON_OFF input.
Drive the ON_OFF input HIGH to transit the module to FULL POWER state. While module enters the Full Power state, Wakeup output goes high. After initialization is complete, an OK-to-Send=TRUE message (`$PSRF150,1*3E`) is output to the host port, indicating that the system firmware is operating and ready to receive commands from the host.

21.1. STARTING THE MODULE

The operational state entered when RESET# is high and ON_OFF is high.
WAKEUP output goes high.
When Vcc is stable, the CPU starts.
On the first transition to the ON state, when supply voltages are first applied or after de-assertion of RESET#, host port configuration inputs on GPIO[7:6] are sampled and copied to internal registers. After initialization is complete, an OK-to-Send=TRUE message is output to the host serial port indicating that the system firmware is operating and ready to receive commands from the host.

Transition of ON_OFF input line from low to high when FSM is ready and in startup-ready state, Hibernate state, standby state, will command the module to start.

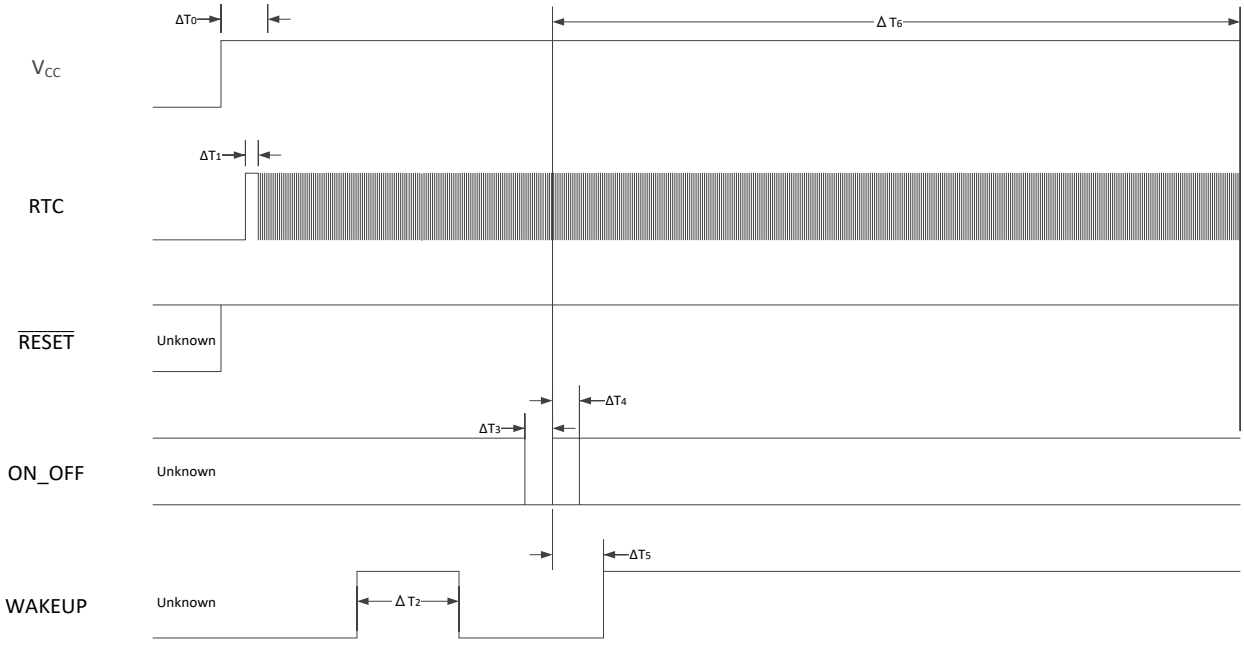


FIGURE 17 – START-UP TIMING

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
f_{RTC}	RTC Frequency	+25°C	-20 ppm	32768	+20 ppm	Hz
t_{RTC}	RTC Tick	+25°C		30.5176		µs
ΔT_1	RTC Startup Time			300		ms
ΔT_0	Power Stabilization		$6 \cdot t_{RTC}+\Delta T_1$	$7 \cdot t_{RTC}+\Delta T_1$	$8 \cdot t_{RTC}+\Delta T_1$	µs
ΔT_2	WAKEUP Pulse	RTC running		10		t_{RTC}
ΔT_3	ON_OFF Low		3			t_{RTC}
ΔT_4	ON_OFF High		3			t_{RTC}
ΔT_5	ON_OFF to WAKEUP high	After ON_OFF		6		t_{RTC}
ΔT_6	ON_OFF to ARM boot	After ON_OFF		2130		t_{RTC}

TABLE 12 – START-UP TIMING

21.2. VERIFYING THE MODULE HAS STARTED

WAKEUP output will go high indicating ORG4572 has started.
System activity indication depends upon selected serial interface.
The first message to come out of module is “OK_TO_SEND” - ‘$PSRF150,1*3E’.

21.2.1. UART

When active, the module will output NMEA messages at the 4800bps.

21.2.2. I²C

In Multi-Master mode with no bus contention - the module will spontaneously send messages.
In Multi-Master mode with bus contention - the module will send messages after the I²C bus contention resolution process allows it to send.

21.2.3. SPI

Since ORG4572 is SPI slave device, there is no possible indication of system “ready” through SPI interface. Host must initiate SPI connection approximately 1s after WAKEUP output goes high.

21.3. CHANGING PROTOCOL AND BAUD RATE[1]

Protocol and baud rate can be changed by NMEA $PSRF100 serial message.

21.4. CHANGING SATELLITE CONSTELLATION[1]

Satellite constellations used in position solution can be changed by OSP® Message ID 222 Sub ID 16.

21.5. SHUTTING DOWN THE MODULE

Transferring module from Full Power state to Hibernate state can be initiated in two ways:

- By a low level input on ON_OFF input.
- By NMEA ($PSRF117) or OSP® (MID205) serial message.

Orderly shutdown process may take anywhere from 10ms to 900ms to complete, depending upon operation in progress and messages pending, and hence is dependent upon serial interface speed and controls. ORG4572 will stay in Full Power state until TX FIFO buffer is emptied.
The last message during shutdown sequence is ‘$PSRF150,0*3F’.

Note:
1. Changes to default firmware settings are volatile and will be discarded at power re-cycle.

22. FIRMWARE

Power On State		On
Default Interface[1]		SPI
SPI Data Format		NMEA
UART Settings		4,800bps.
UART Data Format		NMEA
I²C Settings		Multi-Master 400kbps
I²C Data Format		NMEA
Satellite Constellation		GPS + GLONASS / GPS + BEIDOU
NMEA Messages		$GPGGA @1 sec.
		$GNGNS @ 1 sec.
		$GNGSA @ 1 sec.
		$GPGSV @ 5 sec.
		$GLGSV @ 5 sec.
		$GNRMC @ 1 sec.
Firmware Defaults	SBAS	OFF
	ABP™	OFF
	Static Navigation	ON
	Track Smoothing	OFF
	Jammer Detector	ON
	Jammer Remover	OFF
	Fast Time Sync	OFF
	Pseudo DR Mode	ON
	Power Saving Mode	OFF
	3SV Solution Mode	ON
	MEMS Gateway	OFF
	Data Logger	OFF
	10Hz Update Rate	OFF

TABLE 13 – DEFAULT FIRMWARE SETTINGS

Note:

1. Without external resistors or straps on $\overline{CTS}$ or $\overline{RTS}$.

22.1. FIRMWARE UPDATES

Firmware of ORG4572-R02/R04 is loaded into serial flash. Updated firmware may be provided by OriginGPS as a method of performance improvement. Typical firmware file size is 1100KB. Host controller is initiating load and application of firmware update. SiRFstarV firmware, CCK settings and user applications are always protected in serial flash against corruption of unexpected power removal. SiRFstarV protects all data elements in battery-backed memory and serial flash memory with a CRC-32. All data elements are well protected and recoverable.

23. HANDLING INFORMATION

23.1. MOISTURE SENSITIVITY

ORG4572 modules are MSL 3 designated devices according to IPC/JEDEC J-STD-033B standard.

Module in sample or bulk package should be baked prior to assembly at 125°C for 48 hours.

23.2. ASSEMBLY

The module supports automatic pick-and-place assembly and reflow soldering processes.

Suggested solder paste stencil is 5 mil to ensure sufficient solder volume.

23.3. SOLDERING

Reflow soldering of the module always on component side (Top side) of the host PCB according to standard IPC/JEDEC J-STD-020D for LGA SMD.

Avoid exposure of ORG4572 to face-down reflow soldering process.

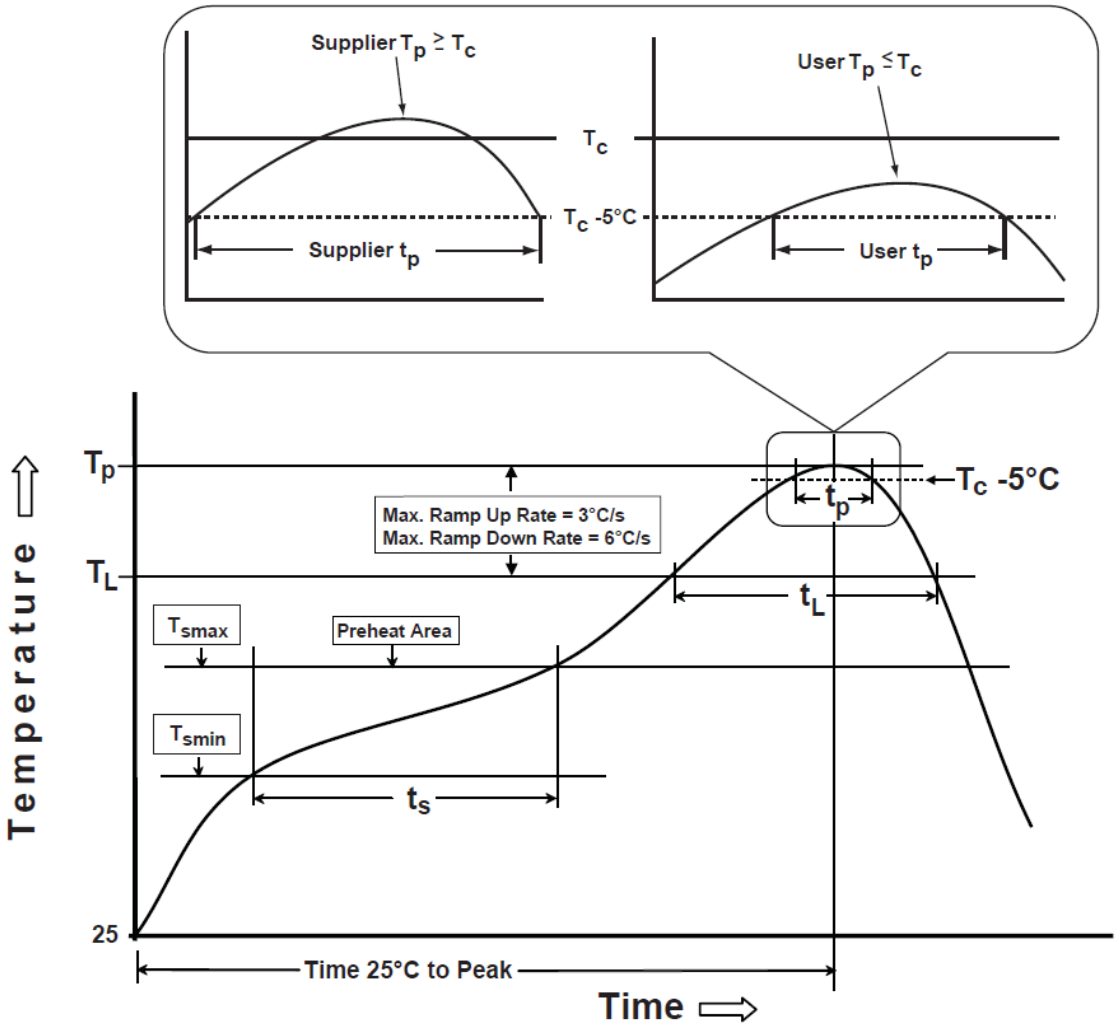


FIGURE 18 – RECOMMENDED SOLDERING PROFILE

Referred temperature is measured on top surface of the package during the entire soldering process.

Suggested peak reflow temperature is 245°C for 30 sec. for Pb-Free solder paste.

Actual board assembly reflow profile must be developed individually per furnace characteristics.

Reflow furnace settings depend on the number of heating/cooling zones, type of solder paste/flux used, board design, component density and packages used.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_C	Classification Temperature		245		°C
T_P	Package Temperature			245	°C
T_L	Liquidous Temperature		217		°C
T_S	Soak/Preheat Temperature	150		200	°C
t_S	Soak/Preheat Time	60		120	s
t_L	Liquidous Time	60		150	s
t_P	Peak Time		30		s

TABLE 14 – SOLDERING PROFILE PARAMETERS

23.4. CLEANING

If flux cleaning is required, module is capable to withstand standard cleaning process in vapor degreaser with the Solvon® n-Propyl Bromide (NPB) solvent and/or washing in DI water.

Avoid cleaning process in ultrasonic degreaser, since specific vibrations may cause performance degradation or destruction of internal circuitry.

23.5. REWORK

If localized heating is required to rework or repair the module, precautionary methods are required to avoid exposure to solder reflow temperatures that can result in permanent damage to the device.

23.6. ESD SENSITIVITY

This product is ESD sensitive device and must be handled with care.

23.7. SAFETY INFORMATION

Improper handling and use can cause permanent damage to the product.

23.8. DISPOSAL INFORMATION

This product must not be treated as household waste.

For more detailed information about recycling electronic components contact your local waste management authority.

24. MECHANICAL SPECIFICATIONS

- ORG4572-R02/R04 module has miniature LGA SMD packaging sized 7mm x 7mm.
- ORG4572-R02/R04 built on a PCB assembly enclosed with metallic RF shield box.
- On bottom side there are 16+4 SMT pads with Cu base and ENIG plating.
- ORG4572-R02/R04 module supports automated pick and place assembly and reflow soldering processes.

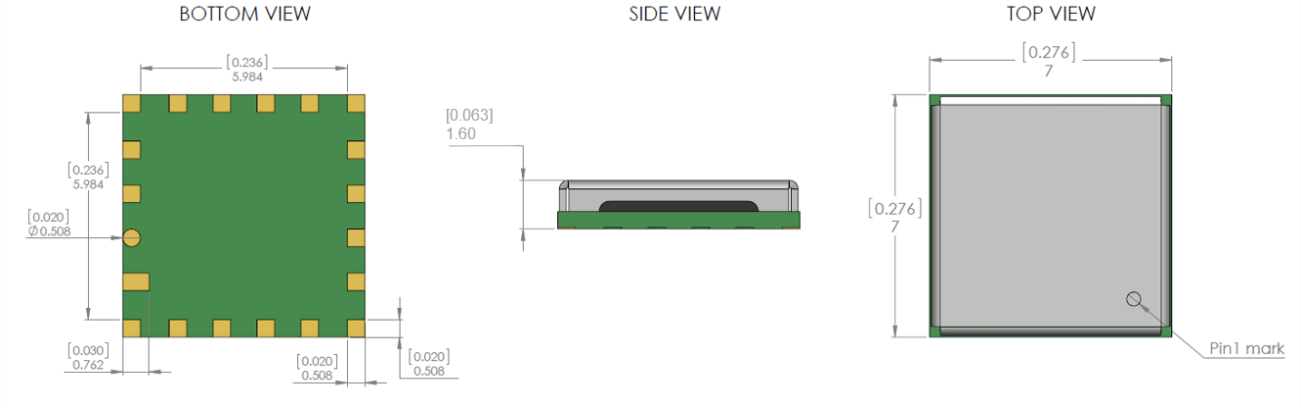


FIGURE 19 – MECHANICAL DRAWING

Dimension	Length	Width	Height	Weight	
mm	7.00 +0.2/ -0.05	7.00 +0.2/ -0.05	1.6 +0.2/ -0.05	gr	0.2
inch	0.276 +0.008/ -0.002	0.276 +0.008/ -0.002	0.063 +0.008/ -0.002	oz	0.01

TABLE 15 – MECHANICAL SUMMARY

25. COMPLIANCE

The following standards are applied on the production of ORG4572-R02/R04 modules:

- IPC-6011/6012 Class2 for PCB manufacturing
- IPC-A-600 Class2 for PCB inspection
- IPC-A-610D Class2 for SMT acceptability

ORG4572-R02/R04 modules are manufactured in ISO 9001:2008 accredited facilities.

ORG4572-R02/R04 modules are manufactured in ISO 14001:2004 accredited facilities.

ORG4572-R02/R04 modules are manufactured in OHSAS 18001:2007 accredited facilities.

ORG4572-R02/R04 modules are designed, manufactured and handled in compliance with the Directive 2011/65/EU of the European Parliament and of the Council of June 2011 on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment, referred as RoHS II.

ORG4572-R02/R04 modules are manufactured and handled in compliance with the applicable substance bans as of Annex XVII of Regulation 1907/2006/EC on Registration, Evaluation, Authorization and Restriction of Chemicals including all amendments and candidate list issued by ECHA, referred as REACH.

ORG4572 modules comply with the following EMC standards:

- EU CE EN55022:06+A1(07), Class B
- US FCC 47CFR Part 15:09, Subpart B, Class B
- JAPAN VCCI V-3/2006.04

26. PACKAGING AND DELIVERY

26.1. APPEARANCE

ORG4572-R02/R04 modules are delivered in reeled tapes for automatic pick and place assembly process.

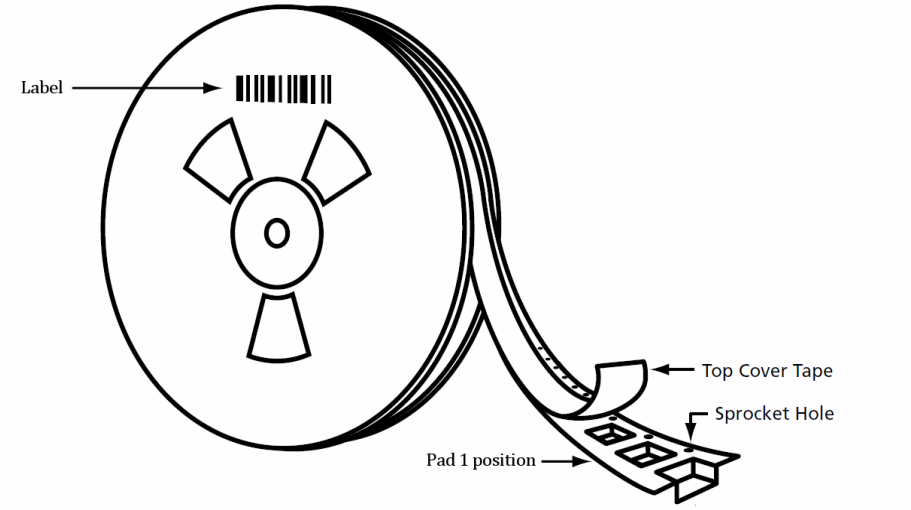


FIGURE 20 – MODULE POSITION

ORG4572-R02/R04 modules are packed in 2 different reel types.

SUFFIX	TR1	TR2
Quantity	500	2000

TABLE 16 – REEL QUANTITY

Reels are dry packed with humidity indicator card and desiccant bag according to IPC/JEDEC J-STD-033B standard for MSL 3 devices.

Reels are vacuum sealed inside anti-static moisture barrier bags.

Sealed reels are labeled with MSD sticker providing information about:

- MSL
- Shelf life
- Reflow soldering peak temperature
- Seal date

Sealed reels are packed inside cartons.

Reels, reel packs and cartons are labeled with sticker providing information about:

- Description
- Part number
- Lot number
- Customer PO number
- Quantity
- Date code

26.2. CARRIER TAPE

Carrier tape material - polystyrene with carbon (PS+C).
Cover tape material – polyester based film with heat activated adhesive coating layer.

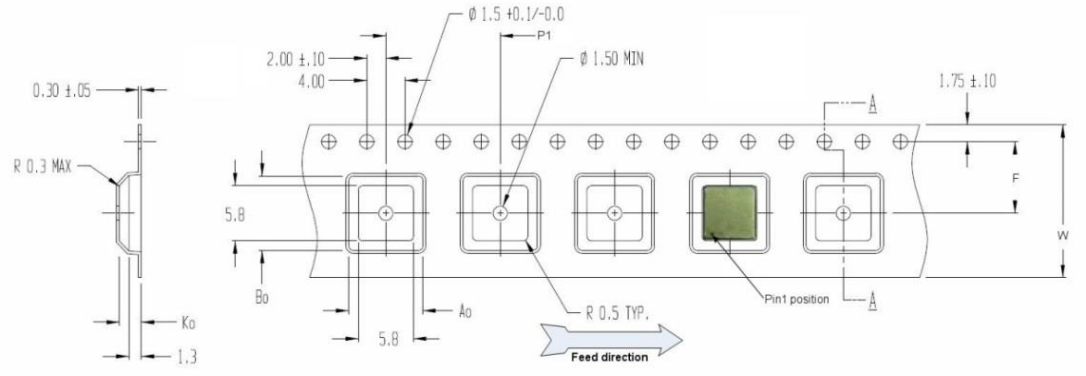


FIGURE 21 – CARRIER TAPE

	mm	inch
A_0	8.3 ± 0.1	0.327 ± 0.004
B_0	8.3 ± 0.1	0.327 ± 0.004
K_0	2.7 ± 0.1	0.106 ± 0.004
F	7.5 ± 0.1	0.295 ± 0.004
P1	12.0 ± 0.1	0.472 ± 0.004
W	16.0 ± 0.3	0.630 ± 0.012

TABLE 17 – CARRIER TAPE DIMENSIONS

26.3. REEL

Reel material - antistatic plastic.

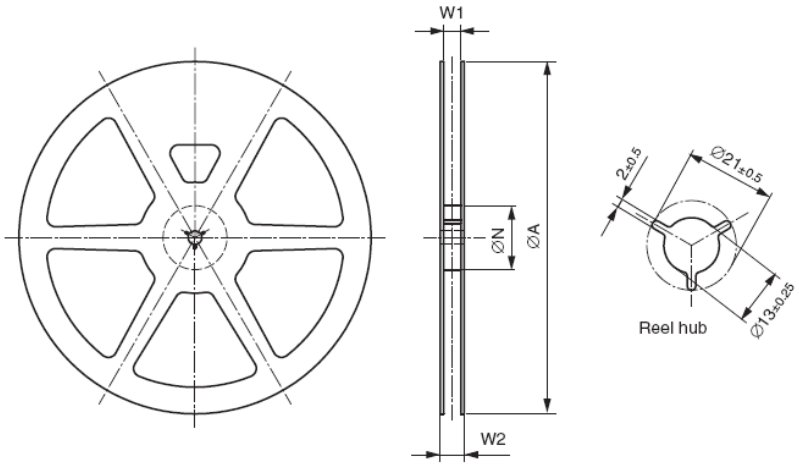


FIGURE 22 – REEL

SUFFIX	TR1		TR2	
	mm	inch	mm	inch
ØA	178.0 ± 1.0	7.00 ± 0.04	330.0 ± 2.0	13.00 ± 0.08
ØN	60.0 ± 1.0	2.36 ± 0.04	102.0 ± 2.0	4.02 ± 0.08
W1	16.7 ± 0.5	0.66 ± 0.02	16.7 ± 0.5	0.66 ± 0.02
W2	19.8 ± 0.5	0.78 ± 0.02	22.2 ± 0.5	0.87 ± 0.02

TABLE 18 – REEL DIMENSIONS

27. ORDERING INFORMATION

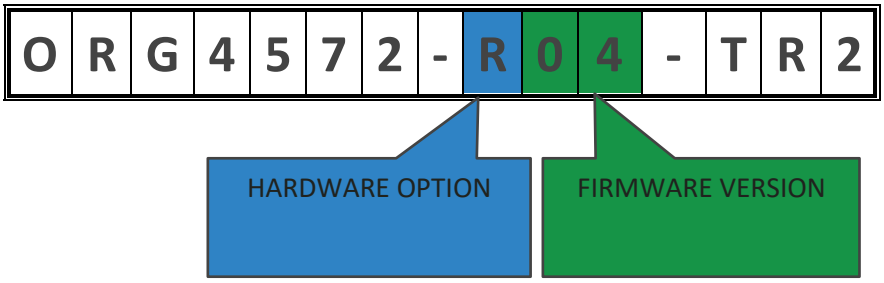


TABLE 19 – ORDERING OPTIONS

PART NUMBER	FW VERSION	HW OPTION	PACKAGING	SPQ
ORG4572-R02-TR1	R	02	REELED TAPE	500
ORG4572-R02-TR2	R	02	REELED TAPE	2000
ORG4572-R02-USB	R	02	GNSS ON A STICK KIT	1
ORG4572-R02-UAR	R	02	EVALUATION KIT	1
ORG4572-R04-TR1	R	04	REELED TAPE	500
ORG4572-R04-TR2	R	04	REELED TAPE	2000
ORG4572-R04-UAR	R	04	EVALUATION KIT	1

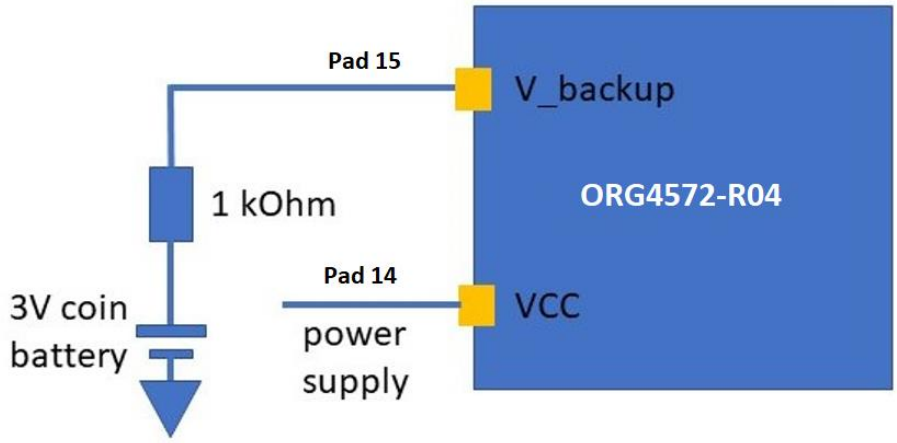
TABLE 20 – ORDERABLE DEVICES

28. APPENDIX 1 – MULTI MICRO HORNET ORG4572-R04

The ORG4572-R04 version has the same features set as the ORG4572-R02, the only difference is that it has an option to connect a coin battery (for example ECR2025 coin battery) to provide power in backup mode. Minimum voltage that the backup battery will support is 2.8V (typical battery 2.8-4.3 V).
With a battery connection, after waking up, the receiver uses:

1. All internal aiding, including RTC time, Ephemeris, and Last Position, resulting in the fastest possible TTFF in either hot or warm start modes.
2. Configuration settings stored in flash after turning power off.

To keep alive the RTC time, the following circuit implementation using a 3V coin battery, can be used. In addition, you need to consider using a charger for the battery or separating the VCC and V_BACKUP with using controlled LDO for each of them.



Important: For regular operation of the module, V_backup input is a must!
In case you don't use a battery, you must connect the V_backup to the VCC.
In this case the VCC must be a typical value of 3.3V instead of 1.8V.
Vio will stay 1.8V TTL.