

ORG4033-MK05

GPS/GNSS Receiver Module

DATASHEET

OriginGPS.com

TABLE OF CONTENTS

1.	About the Spider Family	1
2.	About the ORG4033 Module.....	2
3.	About OriginGPS	3
4.	Module Description	4
4.1.	Module Features.....	4
4.2.	Architecture	5
4.3.	ORG4033 Features Description	7
4.3.1.	Constellation Configuration	7
4.3.2.	1PPS	7
4.3.3.	Static Navigation.....	7
4.3.4.	Assisted GPS (AGPS)	8
4.3.5.	Quasi-Zenith Satellite System (QZSS)	9
4.3.6.	Satellite-Based Augmentation System (SBAS)	9
4.3.7.	Differential GPS (DGPS).....	9
4.3.8.	Jamming Rejection – Active Interference Cancellation (AIC)	10
4.3.9.	Power Management Modes.....	10
4.3.10.	Configuration Settings	13
4.4.	Pads Assignment	14
5.	Mechanical Specifications	16
6.	Electrical Specifications.....	17
6.1.	Absolute Maximum Ratings	17
6.2.	Recommended Operating Conditions	18
7.	Performance	19
7.1.	Acquisition Time	19
7.1.1.	Hot Start	19
7.1.2.	Signal Reacquisition	19
7.1.3.	Aided Start	19
7.1.4.	Warm Start.....	19
7.1.5.	Cold Start	20
7.2.	Sensitivity	20
7.2.1.	Tracking	20
7.2.2.	Reacquisition	20
7.2.3.	Navigation	20



7.2.4.	Hot Start	20
7.2.5.	Aided Start	21
7.2.6.	Cold Start	21
7.3.	Received Signal Strength	21
7.4.	Power Consumption	22
7.5.	Position Accuracy	22
7.6.	Dynamic Constraints	23
8.	Interface	24
8.1.	Power Supply	24
8.1.1.	Nominal VCC = 3.3V	24
8.1.2.	Ground	24
8.2.	Control Interface	24
8.2.1.	UART- Host Interface	24
8.2.2.	I2C	25
8.2.3.	SPI	25
8.3.	Data Interface	26
8.3.1.	Force-On	26
8.3.2.	Reset	26
8.3.3.	1PPS	27
8.3.4.	Wakeup	27
9.	Typical Application Circuit	28
10.	Recommended PCB Layout	29
10.1.	Footprint	29
10.2.	Host PCB	29
10.3.	RF Trace	30
10.4.	PCB Stack-Up	30
10.5.	PCB Layout Restrictions	30
11.	Design Considerations	31
11.1.	Antenna	31
11.2.	RF	31
12.	Commands Description	32
13.	Firmware Updates	33
14.	Handling Information	34
14.1.	Moisture Sensitivity	34
14.2.	Assembly	34
14.3.	Soldering	34
14.4.	Cleaning	36



14.5.	Rework	36
14.6.	ESD Sensitivity	36
14.7.	Safety Information	36
14.8.	Disposal Information.....	36
15.	Compliance.....	37
16.	Packaging and Delivery	38
16.1.	Appearance.....	38
16.2.	Carrier Tape.....	39
16.3.	Reel.....	40
17.	Ordering Information	41
Appendix A. The ORG4033-MK05 Module		42

LIST OF FIGURES

Figure 1. ORG4033 Architecture	5
Figure 2. MT3333 System Block Diagram and Peripheral	6
Figure 3. EASY™ TTFF Timing	8
Figure 4. Periodic Power Saving Mode	11
Figure 5. AlwaysLocate™ Mode: Power vs. Time	12
Figure 6. ORG4033 Top View	15
Figure 7. Mechanical Drawing	16
Figure 8. 1PPS AND UTC	27
Figure 9. Reference Schematic Diagram	28
Figure 10. Footprint	29
Figure 11. Host PCB	29
Figure 12. Typical Microstrip PCB Trace On Fr-4 Substrate.....	30
Figure 13. Typical PCB Stack-Up	30
Figure 14. Recommended Soldering Profile	35
Figure 15. Module Position.....	38
Figure 16. Carrier Tape	39
Figure 17. Reel	40
Figure 18. Ordering Options.....	41
Figure 19. Battery Backup Implementation	42



LIST OF TABLES

Table 1. Related Documentation	x
Table 2. Revision History	x
Table 3. Pin-Out.....	14
Table 4. Mechanical Summary	16
Table 5. Absolute Maximum Ratings.....	17
Table 6. Recommended Operating Conditions	18
Table 7. Acquisition Time	20
Table 8. Sensitivity.....	21
Table 9. Received Signal Strength	21
Table 10. Power Consumption	22
Table 11. ORG4033 Position Accuracy	22
Table 12. Dynamic Constraints.....	23
Table 13. NMEA Input Commands.....	32
Table 14. Soldering Profile Parameters	36
Table 15. Reel Quantity.....	38
Table 16. Carrier Tape Dimensions.....	39
Table 17. Reel Dimensions.....	40
Table 18. Orderable Devices	41

ABBREVIATIONS

Abbreviation	Description
A-GPS	Assisted GPS
AC	Alternating Current
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BPF	Band Pass Filter
C/N ₀	Carrier to Noise density ratio [dB-Hz]
CDM	Charged Device Model
CE	European Community conformity mark
CEP	Circular Error Probability
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CTS	Clear-To-Send
CW	Continuous Wave
DC	Direct Current
DOP	Dilution Of Precision
DR	Dead Reckoning
DSP	Digital Signal Processor
ECEF	Earth Centered Earth Fixed
ECHA	European Chemical Agency
EGNOS	European Geostationary Navigation Overlay Service
EIA	Electronic Industries Alliance
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
ENIG	Electroless Nickel Immersion Gold
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
EU	European Union
EVB	Evaluation Board
EVK	Evaluation Kit
FCC	Federal Communications Commission
FSM	Finite State Machine
GAGAN	GPS Aided Geo-Augmented Navigation
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input or Output
GPS	Global Positioning System
HBM	Human Body Model
HDOP	Horizontal Dilution Of Precision
I ² C	Inter-Integrated Circuit
I/O	Input or Output



Abbreviation	Description
IC	Integrated Circuit
ICD	Interface Control Document
IF	Intermediate Frequency
ISO	International Organization for Standardization
JEDEC	Joint Electron Device Engineering Council
KA	Keep Alive
KF	Kalman Filter
LDO	Low Dropout regulator
LGA	Land Grid Array
LNA	Low Noise Amplifier
LP	Low Power
LS	Least Squares
LSB	Least Significant Bit
MID	Message Identifier
MM	Machine Model
MSAS	Multi-functional Satellite Augmentation System
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
NFZ™	Noise-Free Zones System
NMEA	National Marine Electronics Association
NVM	Non-Volatile Memory
PCB	Printed Circuit Board
PLL	Phase Lock Loop
PMU	Power Management Unit
POR	Power-On Reset
PPS	Pulse Per Second
PRN	Pseudo-Random Noise
PSRR	Power Supply Rejection Ratio
PTF™	Push-To-Fix
QZSS	Quasi-Zenith Satellite System
RAM	Random Access Memory
REACH	Registration, Evaluation, Authorization and Restriction of Chemical substances
RF	Radio Frequency
RHCP	Right-Hand Circular Polarized
RMS	Root Mean Square
RoHS	Restriction of Hazardous Substances directive
ROM	Read-Only Memory
RTC	Real-Time Clock
RTS	Ready-To-Send
SAW	Surface Acoustic Wave
SBAS	Satellite-Based Augmentation Systems
SID	Sub-Identifier



Abbreviation	Description
SIP	System In Package
SMD	Surface Mounted Device
SMPS	Switched Mode Power Supply
SMT	Surface-Mount Technology
SOC	System On Chip
SPI	Serial Peripheral Interface
SV	Satellite Vehicle
TCXO	Temperature-Compensated Crystal Oscillator
TTFF	Time To First Fix
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
VCCI	Voluntary Control Council for Interference by information technology equipment
VEP	Vertical Error Probability
VGA	Variable-Gain Amplifier
WAAS	Wide Area Augmentation System

RELATED DOCUMENTATION

Table 1. Related Documentation

Nº	Document Name
1	ORG4033 Evaluation Kit Datasheet
2	MTK NMEA Manual Packet 3.5
3	Feature List and Command Usage- ORG4033-MK05 and ORG1510MK-05

REVISION HISTORY

Table 2. Revision History

Revision	Date	Change Description	Author
1.0	January 21, 2016	First release	Ori A.
2.0	August 15, 2016	Updated Pin 12 update, backup mode	Mark K.
2.1	August 17, 2016	Updated RESET, WAKEUP	Ori A.
2.2	November 24, 2016	Added Table 8 - Sensitivity test remark.	Mark K.
2.3	February 12, 2017	Updated periodic backup/standby modes	Mark K.
2.4	July 2, 2018	Backup	Gil M.
2.5	July 12, 2018	Pinout	Gil M.
2.6.1	August 5, 2018	Updated section backup mode	Gil M.
2.6.2 / 2.6.3	August 27, 2018	Updated Dynamic constraints / I2C	Gil M.
2.6.4	Dec 12, 2018	Updated P/N MK04 to MK05	Gil M.
2.6.5	Jan 21, 2018	Updated V_BACKUP	Igor M.
2.7	May 19, 2019	Updated schematics, footprint and default constellations which support also Galileo	Igor M.
2.8	May 30, 2019	Data correction	Gil M.
2.9	June 17, 2019	Added standby mode	Gil M.
3.0	September 26, 2019	Updated tolerance for mechanical specifications	Ron T.
3.1	September 19, 2020	Updated Static Navigation Updated I2C Pads	Ron T.
3.2	February 17, 2022	New format, Updated FORCE_ON, V_backup, SPI	Mark R.



SCOPE

This document describes the features and specifications of the ORG1510-MK04/5 GNSS receiver module with integrated antenna.

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SAFETY INFORMATION

Incorrect handling or misuse of the product can cause permanent damage.

This product is an electronic sensitive device (ESD) and must be handled with care.



DISPOSAL INFORMATION

This product must not be treated as household waste.

For more detailed information about recycling electronic components, contact your local waste-management authority.

CONTACT INFORMATION

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1. ABOUT THE SPIDER FAMILY

OriginGPS GNSS receiver modules have been designed to address markets where size, weight, stand-alone operation, highest level of integration, power consumption and design flexibility - all are very important. OriginGPS Spider family breaks size barrier, offering the industry's smallest fully integrated, highly sensitive GPS / GNSS modules.

Spider family features OriginGPS proprietary NFZ™ technology for high sensitivity and noise immunity even under marginal signal condition, commonly found in urban canyons, under dense foliage or when the receiver's position in space rapidly changes.

Spider family enables the shortest TTM (Time-To-Market) with minimal design risks. Just connect an antenna and power supply on a 2-layer PCB.



2. ABOUT THE ORG4033 MODULE

The ORG4033 module is a complete SIP featuring miniature LGA SMT footprint designed to commit unique integration features for high volume cost sensitive applications.

Designed to support compact and traditional applications such as smart watches, wearable devices, asset trackers, the ORG4033 module is a miniature multi-channel GPS, Galileo and GLONASS/ BeiDou, SBAS, QZSS overlay systems receiver that continuously tracks all satellites in view, providing real-time positioning data in industry's standard NMEA format.

The ORG4033 module offers superior sensitivity and outstanding performance, achieving rapid TTFF in less than one second, accuracy of approximately two meters, and tracking sensitivity of -165dBm.

Sized only 5.6mm x 5.6mm, the ORG4033 module is industry's small sized, record-breaking solution.

The ORG4033 module is introducing industry's lowest energy per fix ratio, unparalleled accuracy and extremely fast fixes even under challenging signal conditions, such as in built-up urban areas, dense foliage or even indoor.

Integrated GPS SoC incorporating high-performance microprocessor and sophisticated firmware keeps positioning payload off the host, allowing integration in embedded solutions with low computing resources.

Innovative architecture can detect changes in context, temperature, and satellite signals to achieve a state of near continuous availability by maintaining and opportunistically updating its internal fine time, frequency, and satellite ephemeris data while consuming mere microwatts of battery power.



3. ABOUT ORIGINGPS

OriginGPS develops, manufactures and supplies the world's smallest GNSS and cellular IoT solutions.

Our high-performance miniature GNSS products provide multiple constellation support to help you track everything valuable to you and your business. The OriginIoT™ makes IoT-enabling devices affordable and accessible by eliminating the need for additional embedded software and RF engineering knowhow. The low power cellular IoT system reduces project costs and dramatically shortens time-to-market when you develop cellular IoT devices.

OriginGPS miniature products are ideal for market verticals, such as asset tracking, fleet management, industrial IoT, law enforcement, pet/people tracking, precision agriculture, smart cities, sports and wearables.



4. MODULE DESCRIPTION

This section describes the performance of the ORG4033 module.

4.1. Module Features

- Autonomous operation
- OriginGPS Noise Free Zone System (NFZ™) technology
- Active or Passive antenna support
- Fully integrating:
 - Dual-stage LNA, SAW filter, TCXO, RTC crystal, GNSS SoC, LDO regulator, RF shield, PMU
- Concurrent tracking of multiple constellations
- Uses GPS, Galileo and GLONASS/ BeiDou, QZSS constellations.
- GPS L1 1575.42 frequency, C/A code
- GLONASS L1 FDMA 1598-1606MHz frequency band, SP signal.
- BeiDou B1 1561.098MHz frequency band.
- SBAS (WAAS, EGNOS, MSAS and GAGAN)
- Concurrent tracking of multiple constellations
- DGPS capability
- 99 search channels and 33 simultaneous tracking channels
- Ultra-high Sensitivity down to -165dBm enabling Indoor Tracking
- TTFF of < 1s in 50% of trials under Hot Start conditions
- Low Power Consumption of $\leq 15\text{mW}$
- High Accuracy of < 2.5m in 50% of trials
- AGPS support: Embedded Assist System (EASY) and Extended Prediction Orbit (EPO) and HotStill
- Indoor and outdoor multipath and cross-correlation mitigation
- Jamming Rejection – 12 multi-tone Active Interference Cancellation (AIC)
- 8 Megabit built in flash
- Power management modes: Full Power Continuous, Standby, Periodic and AlwaysLocate™
- NMEA commands and data output over UART serial interface
- High update messages rate of 1,2,5,10Hz
- 1PPS Output
- Static Navigation
- Single voltage supply 3.3V with battery input
- Ultra-small LGA footprint of 5.6mm x 5.6mm
- Ultra-low weight of 0.2g

- Surface Mount Device (SMD)
- Optimized for automatic assembly and reflow equipment
- Operating from -40°C to +85°C
- FCC, CE, VCCI compliant
- RoHS II/REACH compliant

4.2. Architecture

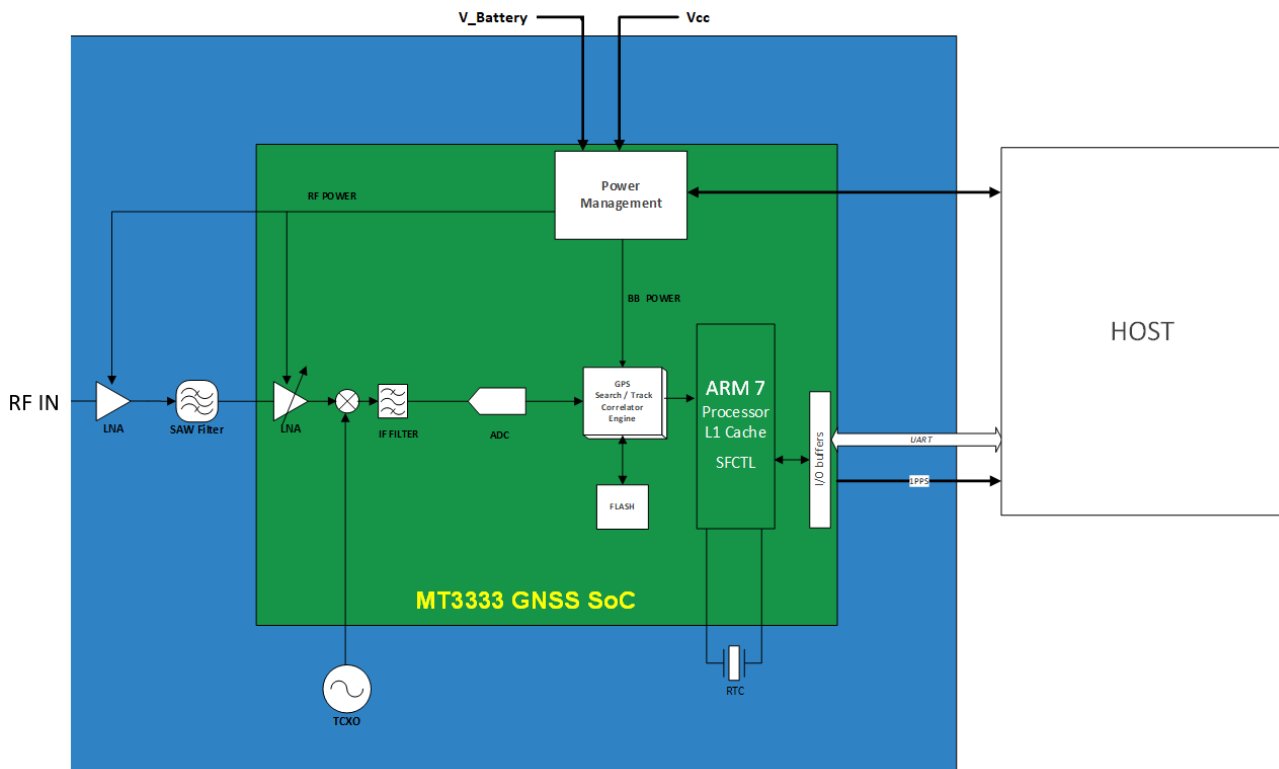


Figure 1. ORG4033 Architecture

• GNSS SAW Filter

Band-Pass SAW filter eliminates out-of-band signals that may interfere to GNSS reception.

GNSS SAW filter is optimized for low Insertion Loss in GNSS band and low Return Loss outside it.

• GNSS LNA

Dual stage cascaded LNAs amplify GNSS signals to meet RF down converter input threshold.

Noise FIGURE optimized design was implemented to provide maximum sensitivity.

• TCXO

Highly stable 26MHz oscillator controls down conversion process in RF block of the GNSS SoC.

Characteristics of this component are important factors for higher sensitivity, shorter TTFF and better navigation stability.

- **RTC crystal**

RTC 32.768 KHz quartz crystal with very tight specifications is necessary for maintaining Hot Start and Warm Start capabilities of the module.

- **MT3333 GNSS SoC**

The MT3333, multi-GNSS System on a Chip designed by MediaTek, which is the world's leading digital media solution provider and largest fab-less IC Company in Taiwan.

It is a hybrid positioning processor that combines GPS, GLONASS, Galileo, BeiDou, SBAS, QZSS, DGPS and AGPS to provide a high-performance navigation solution.

MT3333 is a full SoC built on a low-power RF CMOS, incorporating GNSS RF, GNSS baseband, integrated navigation solution software, ARM® processor and serial flash.

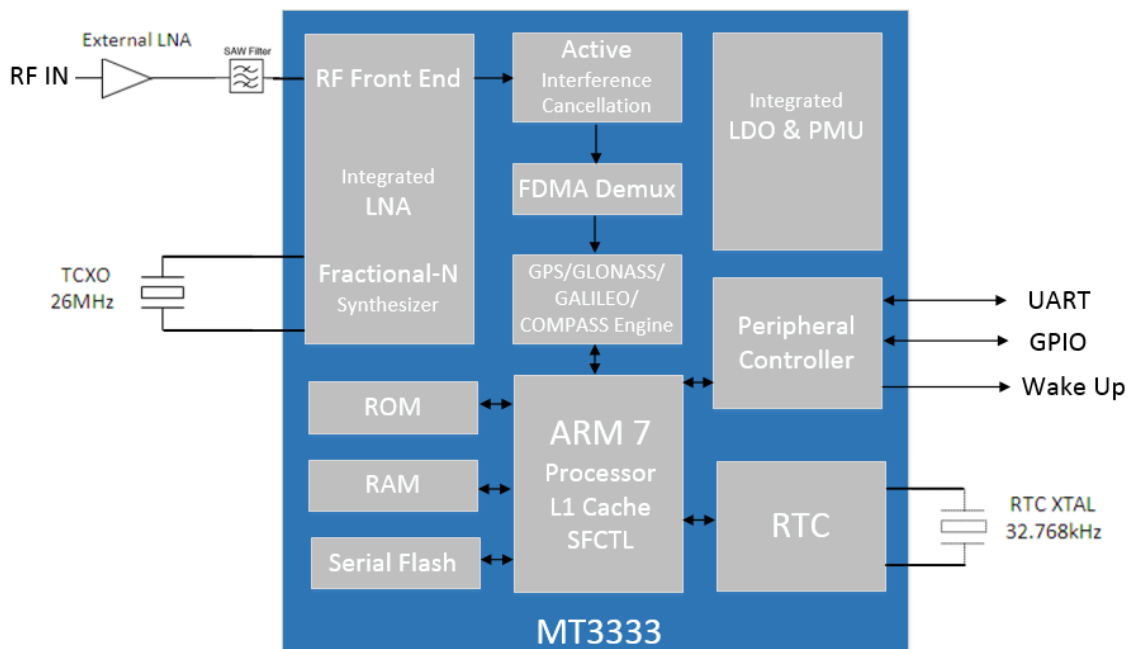


Figure 2. MT3333 System Block Diagram and Peripheral

MT3333 SoC includes the following units:

- GNSS radio subsystem containing single input dual receive paths for concurrent GPS, GLONASS and Galileo or GPS and BEIDO, mixer with current mode interface between the mixer and multi-modes low pass filter, fractional-N synthesizer, integrated self-calibrating filters, IF VGA with AGC, high-sample rate ADCs with adaptive dynamic range.
- Measurement subsystem including DSP core for GNSS signals acquisition and tracking, interference scanner and detector, interference removers, multipath and cross-correlation detectors, dedicated DSP code ROM and DSP cache RAM.
- Measurement subsystem interfaces GNSS radio subsystem.

- Navigation subsystem comprising ARM7® microprocessor system for position, velocity and time solution, program ROM, data RAM, cache and patch RAM and SPI flash.
- Peripheral Controller subsystem containing UART Host interface, RTC block, wake up signal option, and GPIO.
- Peripheral Controller subsystem interfaces navigation subsystem, PLL and PMU subsystems.
- Navigation subsystem interfaces measurement subsystem.
- PMU subsystem containing voltage regulators for RF and baseband domains.

4.3. ORG4033 Features Description

This section describes the features of the ORG4033 module.

4.3.1. Constellation Configuration

- GPS, GLONASS and Galileo - default
- GPS and BeiDou - available

4.3.2. 1PPS

1PPS (Pulse Per Second) may be selected to be outputted in one the following configurations:

- Output PPS in either 2D or 3D fix mode
- Output PPS only in 3D fix mode
- Output PPS After the first Fix
- Always output PPS - default configuration

The following features may be configured via a command:

- Pulse duration
- Pulse frequency
- Active high or active low pulse

The pulse may vary $\pm 30\text{ns}$ (1σ). There is no correlation between the PPS signal and the UTC.

4.3.3. Static Navigation

Static Navigation is an operational mode in which the receiver will freeze the position fix when the speed falls below a threshold (indicating that the receiver is stationary). The course is also frozen, and the speed is reported as 0. The navigation solution is then unfrozen when the speed increases above a threshold. The speed threshold can be set via a command (PMTK 386).

Static Navigation is disabled by default but can be enabled by command. This feature is useful for applications in which very low dynamics are not expected, the classic example being an automotive application.

4.3.4. Assisted GPS (AGPS)

Assisted GPS (or Aided GPS) is a method by which TTFF is reduced using information from a source other than broadcast GPS signals. The necessary ephemeris data is calculated either by the receiver itself (locally generated ephemeris) or a server (server-generated ephemeris) and stored in the module.

ORG4033 has EASY, EPO and HotStill technology to allow for Hot Starts even in weak signal conditions. EPO (Extended Prediction Orbit) is one of MediaTek's innovative proprietary off-line server based AGPS solution. Host could use an application to store and load the EPO files into device. With multi-constellation EPO, the user experience will be enhanced by the improved Time To First Fix (TTFF) and better first fix accuracy.

4.3.4.1. Locally-generated AGPS (Embedded Assist System – EASY)

Easy is the abbreviation of Embedded Assist System. The benefits of using this feature are:

- EASY works as embedded software which accelerates TTFF by predicting satellite navigation messages from received Ephemeris
- No additional computing interval for EASY task. EASY is efficiently scheduled and computed during GPS workflow.
- World leading technology with no additional design – in efforts.

Up to 3 days extension for single received ephemeris:

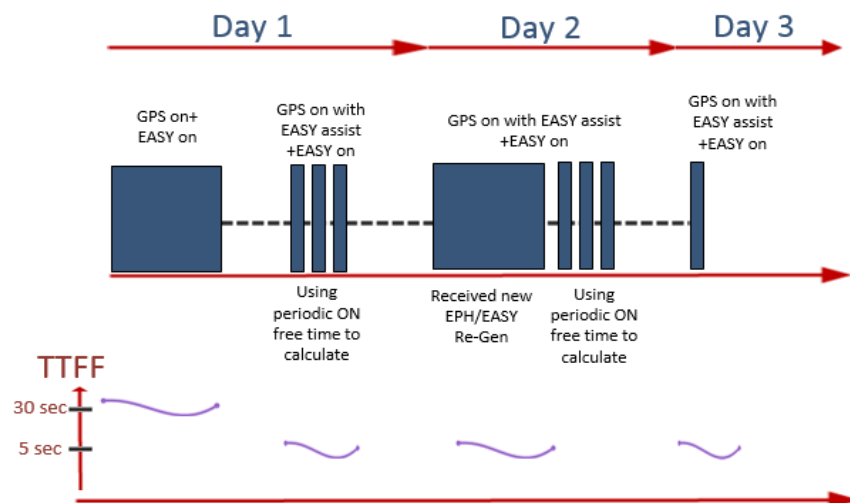


Figure 3. EASY™ TTFF Timing



4.3.4.2. Server-generated AGPS (Extended Prediction Orbit – EPO)

The AGPS (EPO™) supply the predicated Extended Prediction Orbit data to speed TTFF ,users can download the EPO data to GNSS engine from the FTP server by internet or wireless network ,the GNSS engine will use the EPO data to assist position calculation when the navigation information of satellites are not enough or weak signal zone .

Host could use an application to store and load the EPO files into device. With multi-constellation EPO, the user experience will be enhanced by the improved Time To First Fix (TTFF) and better first fix accuracy.

The predicted ephemeris file is obtained from the AGPS server and is injected into the module over serial port 1 (RX1). These predictions do not require local broadcast ephemeris collection, and they are valid for up to 14 days.

4.3.4.3. HotStill (Extended Prediction Orbit)

HotStill is one of MTK's innovative proprietary Off-line client-based A-GPS solution which could greatly accelerate GPS TTFF (Time to First Fix) in urban canyon or weak signal environment from several minutes to only few seconds. It works as a background software running on the host processor to predicate satellite orbit navigation data and generate Broadcast Ephemeris Extension (BEE) from received broadcast ephemeris as well as no network connection requirements. Hotstill feature is designed for use on smartphones and it's not suitable for standalone designs.

4.3.5. Quasi-Zenith Satellite System (QZSS)

The three satellites of the Japanese SBAS are in a highly inclined elliptical orbit which is geosynchronous (not geostationary) and has analemma-like ground tracks. This orbit allows continuous coverage over Japan using only three satellites. Their primary purpose is to provide augmentation to the GPS system, but the signals may also be used for ranging. NMEA reporting for QZSS may be enabled/disabled by the user.

4.3.6. Satellite-Based Augmentation System (SBAS)

The ORG4033-MK05 receiver is capable of using Satellite-Based Augmentation System (SBAS) satellites as a source of both differential corrections and satellite range measurements. These systems (WAAS, EGNOS, MSAS, and GAGAN) use geostationary satellites to transmit regional differential corrections via a GNSS-compatible signal. The use of SBAS corrections can significantly improve position accuracy and is enabled by default.

4.3.7. Differential GPS (DGPS)

DGPS is a Ground-Based Augmentation System (GBAS) for reducing position errors by applying corrections from a set of accurately surveyed ground stations located over a wide area. These reference stations measure the range to each satellite and compare it to the known-good range. The differences can then be used to compute a set of corrections which are transmitted to a DGPS receiver, either by radio or over the internet. The DGPS receiver can then send them to the serial port 1 (RX1) using

the RTCM SC-104 message protocol. The corrections can significantly improve the accuracy of the position reported to the user. The receiver can accept and apply either the RTCM SC-104 messages or SBAS differential data.

4.3.8. Jamming Rejection – Active Interference Cancellation (AIC)

The ORG4033 detect, track and removes narrow-band interfering signals (jamming signals) without the need for external components or tuning. It tracks and removes up to 12 CW (Continuous Wave) type signals up to -80 dBm (total power signal levels). By default, the jamming detection is enabled but can be disabled by command. This feature is useful both in the design stage and during the production stage for uncovering issues related to unexpected jamming. When enabled, AIC will increase current consumption by about 1 mA. Impact on GNSS performance is minimal at low jamming levels, however at high jamming levels (e.g., -90 to -80 dBm), the RF signal sampling ADC starts to become saturated after which the GNSS signal levels start to diminish.

4.3.9. Power Management Modes

The ORG4033 support operational modes that allow them to provide positioning information at reduced overall current consumption. Availability of GNSS signals in the operating environment will also be a factor in choice of power management modes. The designer can choose a mode that provides the best trade-off of performance versus power consumption.

The power management modes are described below, and can be enabled via command:

- Full Power Continuous- for best GNSS performance
- Power save mode to optimize power consumption:
 - ♦ Standby
 - ♦ Periodic
 - ♦ AlwaysLocate™

4.3.9.1. Full Power Continuous Mode

The modules start up in full power continuous mode. This mode uses the acquisition engine at full performance resulting in the shortest possible TTFF and the highest sensitivity. It searches for all possible satellites. The receiver then switches to the tracking engine to lower the power consumption when:

- A valid GPS/GNSS position is obtained
- The ephemeris for each satellite in view is valid

To return to Full Power mode (from a low power mode, excluding Backup mode), send the following command: **PMTK225,0** [Just after the module wakes up from its previous sleep cycle].

4.3.9.2. Standby Mode

In this mode, the receiver stops navigation, the internal processor enters standby state, and the current drain at main supply (VCC) is reduced. Standby mode is entered by sending one of the following commands:

PMTK161,0 - Standby stop mode = Turn off VTCXO, RF a, baseband.

PMTK161,1 - Standby sleep mode = Turn off RF and baseband.

The host can then wake up the module from Standby mode to Full Power mode by sending any byte to the serial port.

4.3.9.3. Periodic Mode

This mode allows autonomous power on/off with reduced fix rate to reduce average power consumption. In periodic mode, the main power supply VCC is still powered, but power distribution to internal circuits is controlled by the receiver.

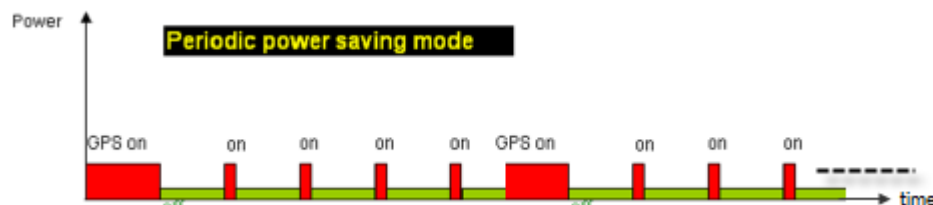


Figure 4. Periodic Power Saving Mode

Enter periodic mode by sending the following command:

PMTK225,<Type>,<Run_time>,<Sleep_time>,<2nd_run_time>,<2nd_sleep_time>*<checksum>

Where:

- Type = 1 for Periodic backup mode
- Type = 2 for Periodic standby mode
- Run_time = Full Power period (ms)
- Sleep_time = Standby period (ms)
- 2nd_run_time = Full Power period (ms) for extended acquisition if GNSS acquisition fails during Run_time.
- 2nd_sleep_time = Standby period (ms) for extended sleep if GNSS acquisition fails during Run_time

Example: **PMTK225,2,3000,12000,18000,72000**

for periodic mode with 3 s navigation and 12 s sleep. The acknowledgement response for this command is: **PMTK001,225,3**

Periodic mode is exited and switched back to Full Power Continuous Mode by sending the command: **PMTK225,0**

just after the module wakes up from a previous sleep cycle.

4.3.9.4. AlwaysLocate™ Mode

AlwaysLocate™ is an intelligent controller of the Periodic mode; the main power supply VCC is still powered up, but power distribution is internally controlled. Depending on the environment and motion conditions, the module can autonomously and adaptively adjust the parameters of the Periodic mode, e.g., ON/OFF ratio and fix rate to achieve a balance in positioning accuracy and power consumption. The average current can vary based on conditions.

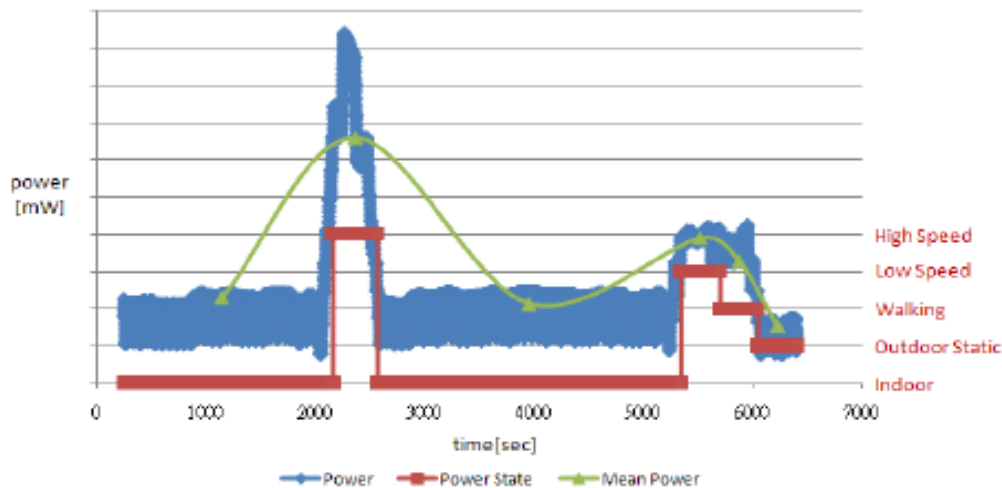


Figure 5. AlwaysLocate™ Mode: Power vs. Time

Enter AlwaysLocate™ mode by sending the following NMEA command:
PMTK225,<mode>*<checksum><CR><LF>

Where: mode=9 for AlwaysLocate™

Example:

PMTK225,9

The acknowledgement response for the command is:

PMTK001,225,3

The user can exit low power modes to Full Power by sending NMEA command:

PMTK225,0

Just after the module wakes up from its previous sleep cycle.

4.3.9.5. Backup Mode

Backup Mode means a low quiescent power state where receiver operation is stopped.

V_backup is powered on, but the current consumption is minimal.

After waking up, the receiver uses all internal aiding, including GNSS time, Ephemeris, and Last Position, resulting in the fastest possible TTFF in either hot or warm start modes. During Backup State, the I/O block is powered off. The suggestion is that the host forces its outputs to a low state or to a high-Z state during the Backup State to minimize small leakage currents at receiver's input signals.

The Current consumption is ~12uA in BACKUP mode (VCC & V_BACKUP).



To Enter Backup Mode:

There are two options to enter the backup mode.

Option 1

The backup mode can be entered with the NMEA software command – PMTK225,4 (+checksum).

Important: Before sending the command the FORCE_ON pin must be tied to ground.

While in Backup mode, the module will consume ~12uA from VCC & V_BACKUP.

In case the command is sent while the FORCE_ON is not tied to the ground – the module would get into idle state, but not BACKUP mode, and the current consumption would be significantly higher.

The Current consumption is ~12uA in BACKUP mode while FORCE_ON pin of module is tied to ground with jumper. In real cases FORCE_ON pin is grounded by active device with residue resistance differ from zero so current consumption may be 2-3 times higher i.e., 25uA.

FORCE_ON must be tied to ground if you need to stay in BACKUP mode.

Example:

PMTK225,4 Enter backup mode

NMEA Return feedback:

PMTK001,225,3

Module will stay in BACKUP mode while FORCE ON is tied to ground.

To Exit from BACKUP mode, disconnect FORCE_ON from ground and pull the FORCE_On to high

level, wait about 1 sec and then release it to logic low again.

Important: It is not possible to wake up the module from backup mode by software command.

Option 2

The backup mode can be entered by disconnecting the VCC.

Connect the V_backup to an external battery, and then disconnect the VCC from the module. The module will now enter the backup mode.

To return to Full Power, reconnect the VCC and the module will switch to the active state and acquire a hot start.

During this process, make sure to keep the FORCE_ON pin at a low level.

4.3.10. Configuration Settings

Currently, the configuration settings will be erased after turning down the power.

Be aware to this issue on power cycles while shutting down the module.



4.4. Pads Assignment

Table 3. Pin-Out

Pad	Name	Function	Direction	Logic Level
1	1PPS	UTC Time Mark	Output	2.8V
2	RX	UART Receive (Serial Input)	Input	2.8V
3	TX	UART Transmit (Serial Output)	Output	2.8V
4	GND	System Ground	Power	
5	RF IN	RF input	Input	50Ω
6	GND	System Ground	Input power	
7	CTS	UART Clear To Send/ I2C Clock	Input	2.8V
8	RTS	UART Ready To Send/ I2C Data	Output	2.8V
9	FIX LED	FIX LED indicator	Output	2.8V
10	GND	System Ground		
11	FORCE ON	Forced full-power mode signal – Active Low	Input	2.8V
12	V_ BACKUP	Input for battery backup	Input power	2.8-4.2V
13	NC	Do not connect		
14	WAKEUP	WAKEUP	Output	2.8V
15	V _{CC}	System Power	Power	3.3V
16	GND	System Ground	Power	
17	$\overline{\text{RESET}}$	System Reset– Active Low	Input	2.8V
18	NC	spare		

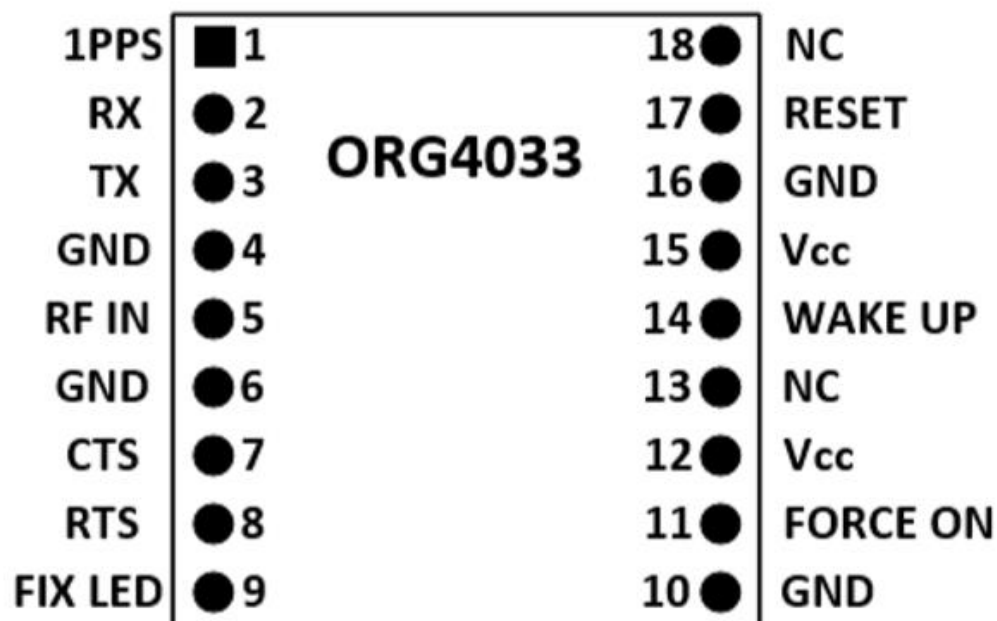


Figure 6. ORG4033 Top View

5. MECHANICAL SPECIFICATIONS

- ORG4033 module has advanced ultra-miniature LGA SMD packaging sized 5.6mm x 5.6mm.
- ORG4033 built on a PCB assembly enclosed with metallic RF shield box.
- There are 18 LGA SMT pads made Cu base and ENIG plating on bottom side.

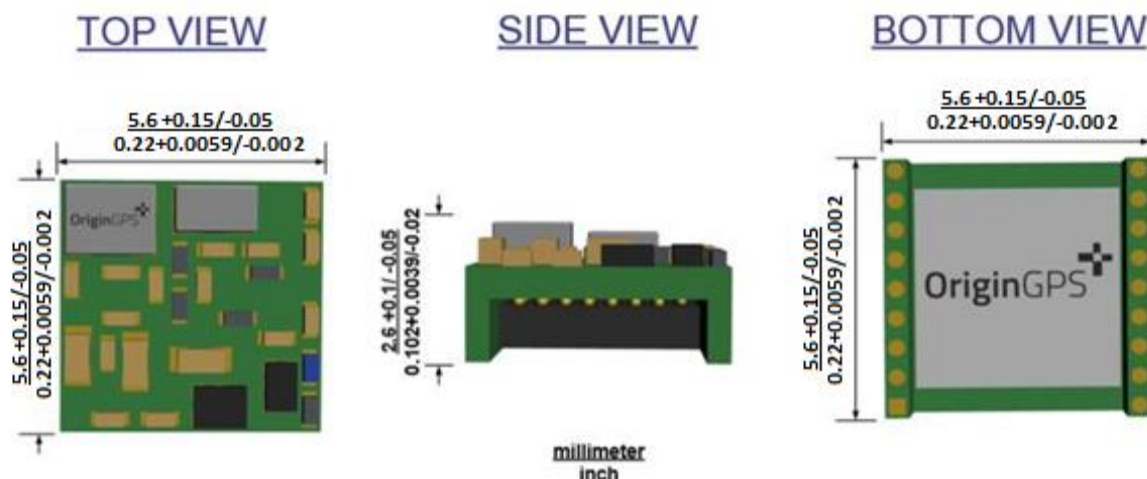


Figure 7. Mechanical Drawing

Table 4. Mechanical Summary

Dimensions	Length	Width	Height	Weight	
mm	5.6 +0.15/ -0.05	5.6 +0.15/ -0.05	2.6 +0.1/ -0.05	gr	0.2
inch	0.22 +0.0059/ -0.002	0.22 +0.0059/ -0.002	0.102 +0.004/ -0.002	oz	0.008



6. ELECTRICAL SPECIFICATIONS

This section describes the electrical specifications of the ORG4033 module.

6.1. Absolute Maximum Ratings

Stresses exceeding Absolute Maximum Ratings may damage the device.

Table 5. Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Unit
Power Supply Voltage		V _{CC}	-0.30	+4.3	V
Backup Battery Supply Voltage		V _{backup}	-0.30	+4.3	V
Power Supply Current ¹		I _{CC}		120	mA
RF Input Voltage ²		V _{RF}	-0.30	+3.6	V
I/O Voltage		V _{IO}	-0.30	+3.6	V
I/O Source/Sink Current		I _{IO}		+8	mA
ESD Voltage		V _{IO/RF, HBM Model} ³	(-/+) 1000	(-/+) 3000	V
		V _{IO/RF, MM Model} ⁴	(-/+) 100	(-/+) 300	V
RF Power ⁵	f _{IN} = 1560MHz÷1630MHz	P _{RF}		+10	dBm
	f _{IN} <1560MHz, >1630MHz			+30	dBm
Operating Temperature		T _{AMB}	-45	+90	°C
Storage Temperature		T _{ST}	-50	+125	°C
Lead Temperature ⁶		T _{LEAD}	-5	+260	°C

- Note:**
1. Inrush current of up to 100mA for about 20μs duration.
 2. Voltage applied on antenna element.
 3. Human Body Model (HBM) contact discharge per EIA/JEDEC JESD22-A114D. Step: 500V (+/-).
 4. Machine Model (MM) contact discharge per EIA/JEDEC JESD22-A115C. Step: 50V (+/-).
 5. Power delivered to antenna element.
 6. Lead temperature at 1mm from case for 10s duration.



6.2. Recommended Operating Conditions

Exposure to stresses above Recommended Operating Conditions may affect device reliability.

Table 6. Recommended Operating Conditions

Parameter	Symbol	Mode / pad	Test Conditions	Min	Typ	Max	Unit
Power supply voltage	V _{CC}	V _{CC}		+3.00	+3.3	+3.60	V
Backup Battery supply voltage	V _{backup}	V _{backup}		+2.80	+3.60	+4.20	V
Digital IO Pin Low level input voltage	V _{IL}			-0.3		+0.7	V
Digital IO Pin High level input voltage	V _{IH}			+2.1		+3.6	V
Digital IO Pin Low level output voltage	V _{OL}		I _{OL} =2mA	-0.3		+0.4	V
Digital IO Pin High level output voltage	V _{OH}		I _{OH} =2mA	+2.4	+2.8	+3.1	V
Power Supply Current ¹	I _{CC}	Acquisition	GPS		40		mA
			GPS+GLONASS		45		mA
		Tracking	GPS		28		mA
			GPS+GLONASS		35		mA
		Standby			0.5		mA
		Backup		7	12	25	μA
Input Impedance	Z _{IN}	RF Input	f _{IN} = 1575.5MHz		50		Ω
Input Return Loss	R _{LIN}			-7			dB
Input Power Range	P _{IN}		GPS or GLONASS	-165		-110	dBm
Input Frequency Range	f _{IN}			1560		1607	MHz
Operating Temperature	T _{AMB}			-40	+25	+85	°C
Storage Temperature ²	T _{ST}			-50	+25	+125	°C
Relative Humidity ³	R _H		T _{AMB}	5		95	%

- Note:**
1. Typical values under signal conditions of -130dBm and ambient temperature of +25°C and low gain configuration. Tested on the EVB with 12x12mm passive antenna
 2. Longer TTFF is expected while operating below -30°C to -40°C.
 3. Relative Humidity is within Operating Temperature range.



7. PERFORMANCE

This section describes the performance of the ORG4033 module.

7.1. Acquisition Time

TTFF (Time To First Fix) – is the period of time from module's power-up till valid position estimation.

7.1.1. Hot Start

Hot Start results either from a software reset after a period of continuous navigation or a return from a short idle period that was preceded by a period of continuous navigation.

During Hot Start all critical data (position, velocity, time, and satellite ephemeris) is valid to the specified accuracy and available in RAM.

7.1.2. Signal Reacquisition

Reacquisition follows temporary blocking of GNSS signals.

Typical reacquisition scenario includes driving through tunnel.

7.1.3. Aided Start

Aided Start is a method of effectively reducing TTFF by providing valid satellite ephemeris data.

Aiding can be implemented using Embedded Assist System (EASY) and Extended Prediction Orbit (EPO) and HotStill

7.1.4. Warm Start

Warm Start typically results from user-supplied position and time initialization data or continuous RTC operation with an accurate last known position available in RAM.

In this state position and time data are present and valid, but satellite ephemeris data validity has expired.



7.1.5. Cold Start

Cold Start occurs when satellite ephemeris data, position and time data are unknown. Typical Cold Start scenario includes first power application.

Table 7. Acquisition Time

Operation ¹	Mode	Value	Unit
Hot Start		< 1	s
Aided Start ³		< 3	s
Warm Start	GPS + GLONASS	< 26	s
	GPS	< 29	s
Cold Start	GPS + GLONASS	< 23	s
	GPS	< 31	s
Signal Reacquisition ²		< 3	s

- Note:**
1. EVK is 24-hrs. Static under signal conditions of -130dBm and ambient temperature of +25°C.
 2. Outage duration ≤ 30s.
 3. Dependent on aiding data connection speed and latency
 4. Tested on the EVB with 12x12mm passive antenna

7.2. Sensitivity

This section describes the sensitivity of the ORG4033 module.

7.2.1. Tracking

Tracking is an ability of receiver to maintain valid satellite ephemeris data.

During tracking receiver may stop output valid position solutions.

Tracking sensitivity defined as minimum GNSS signal power required for tracking.

7.2.2. Reacquisition

Reacquisition follows temporary blocking of GNSS signals.

Reacquisition sensitivity defined as minimum GNSS signal power required for reacquisition.

7.2.3. Navigation

During navigation receiver consequently, outputs valid position solutions.

Navigation sensitivity defined as minimum GNSS signal power required for reliable navigation.

7.2.4. Hot Start

Hot Start sensitivity defined as minimum GNSS signal power required for valid position solution under Hot Start conditions.



7.2.5. Aided Start

Aided Start sensitivity defined as minimum GNSS signal power required for valid position solution following aiding process.

7.2.6. Cold Start

Cold Start sensitivity defined as minimum GNSS signal power required for valid position solution under ColdStart conditions, sometimes referred as ephemeris decode threshold.

Table 8. Sensitivity

Operation ¹	Mode	Value	Unit
Tracking	GPS	-165	dBm
	GLONASS	-165	dBm
Navigation	GPS	-163	dBm
	GLONASS	-163	dBm
Reacquisition ²	GPS+GLONASS	-160	dBm
Hot Start	GPS+GLONASS	-163	dBm
Aided Start	GPS+GLONASS	-160	dBm
Cold Start	GPS+GLONASS	-148	dBm

** The above values have been tested at update rate of 1 Hz. While working in a higher update rate there is some signal degradation.

7.3. Received Signal Strength

Table 9. Received Signal Strength

Parameter ⁴	Value	Unit
C/N ₀	45	dB-Hz

- Note:**
1. EVK is static, ambient temperature is +25°C, RF signals are conducted
 2. Outage duration ≤ 30s.
 3. Aiding using Broadcast Ephemeris (Ephemeris Push™) or Extended Ephemeris (CGEE™ or SGEE™).
 4. Average C/N₀ reported for 4 SVs, EVK is 24-hrs. Static, outdoor, ambient temperature is +25°C.



7.4. Power Consumption

Table 10. Power Consumption

Operation ¹	Mode	Value	Unit
Acquisition	GPS	132	mW
	GPS + GLONASS	148.5	mW
Tracking	GPS	92.4	mW
	GPS + GLONASS	115.5	mW
Standby state		1.65	mW
Backup state		39.6	uW

Note: 1. Typical values under conducted signal conditions of -130dBm and ambient temperature of +25°C.
Measured voltage= 3.28V.

7.5. Position Accuracy

Table 11. ORG4033 Position Accuracy

Parameter	Constellation	CEP (m)
Horizontal Position Accuracy	GPS	2.5
Horizontal Position Accuracy	GLONASS	2.6
Horizontal Position Accuracy	BeiDou	10.2
Horizontal Position Accuracy	GPS + GLONASS	2.5
Horizontal Position Accuracy	GPS + BeiDou	2.5

Note: 1. Module is static under signal conditions of -130dBm, ambient temperature is +25°C.
2. EVK is 24-hrs. Static, ambient temperature is +25°C.
3. Speed over ground $\leq 30\text{m/s}$.



7.6. Dynamic Constraints

Table 12. Dynamic Constraints

Parameter	Metric	Imperial
Velocity	515m/s	1,000knots
Altitude	10000m	32808 ft
Altitude Balloon mode	80000m	262467 ft
Acceleration	4g	

Note: 1. Standard dynamic constraints according to regulatory limitations.



8. INTERFACE

This section describes the general interface of the ORG4033 module.

8.1. Power Supply

It is recommended to keep the power supply on all the time in order to maintain RTC block active and keep satellite data in RAM for fastest possible TTFF. When V_{CC} is removed settings are reset to factory default and the receiver performs Cold Start on next power up.

8.1.1. Nominal VCC = 3.3V

V_{CC} is 3.3v DC and must be provided from regulated power supply.

During tracking the processing is less intense compared to acquisition, therefore power consumption is lower.

Filtering is important to manage high alternating current flows on the power input connection. An additional LC filter on ORG4033 power input may be needed to reduce system noise.

The high rate of ORG4033 input current change requires low ESR bypass capacitors. Additional higher ESR output capacitors can provide input stability damping.

The ESR and size of the output capacitors directly define the output ripple voltage with a given inductor size. Large low ESR output capacitors are beneficial for low noise. Voltage ripple below 40mVPP is allowed. Higher voltage ripple may compromise ORG4033 performance.

8.1.2. Ground

Ground pad must be connected to host PCB Ground with shortest possible trace or by multiple VIAs.

8.2. Control Interface

ORG4033-MK05 has a three host interfaces: UART, I2C and SPI.

The switching between the interfaces is by firmware update.

8.2.1. UART- Host Interface

The ORG4033 module has standard UART ports:

8.2.1.1. TX

TX used for GPS data reports. Output logic high voltage level is 2.8V.

The TX serial data line outputs NMEA serial data at a default bit rate of 9600 bps.

When no serial data is being output the TX data line idles high.



8.2.1.2. RX

RX used for receiver control. Input logic high voltage level is 2.8V.

The RX data line accepts NMEA commands at a default bit rate of 9600 bps.

When the receiver is powered down, do not back drive this or any other GPIO line.

The idle state for serial data from the host computer is logic 1.

8.2.2. I2C

I2C interface is enabled by default starting from F.W version 5.1.1.

I2C host interface features are:

- I2C Slave mode – host initiates clock and data, operating speed 400kbps.
- ORG4033-mk support 7 bit I2C address.
- I2C default slave address '0x10'.
- Individual Tx FIFO buffer length of 255 bytes. Master can read one I2C data packet of max. 255 bytes at a time.
- In order to read entire NMEA packet of one second, master need to read several I2C data packets and extract valid NMEA data. After reading one I2C data packet, sleep 2ms before reading the next packet. In case entire packet of 1 second was read, wait for a longer period for the next NMEA packet.

8.2.3. SPI

The ORG4033-MK05 will work in a slave mode, while the master can read one SPI data packet with 255 bytes max. each time.

- To read one NMEA packet, the master should send padding bytes ("0xFF") for receiving NMEA data from the slave
- To read the entire NMEA packet of one second, the master should read several SPI data packets and extract valid NMEA data from them.
- Baud rate is up to 700kbit/s

for more detailed information, please refer to "MTK_SPI application notes" document.

Note: the ORG4033-MK05 with SPI option has a different part number. Please refer to the "Ordering information" (section 15)



8.3. Data Interface

This section describes the data interface of the ORG4033 module.

8.3.1. Force-On

FORCE-ON is an input pin which controls the power states of the module.

There are two possible states for this pin – LOW and HIGH.

LOW state:

If we run the command “PMTK225,4”, the module will enter a Backup mode. In this mode, the module enters the lowest power consumption mode.

*Return to full power mode:

- Set FORCE_ON to HIGH
- Wait 1sec
- Set FORCE_ON to LOW

If we run the command “PMTK225,1,...”, the module will enter a periodic backup mode.

*Return to full power mode:

- Set FORCE_ON to HIGH
- Run command “PMTK225,0”
- Wait for 100ms
- Set FORCE_ON to LOW

HIGH state:

- Note - in this state, the module can't enter a backup mode.
- If we run the command “PMTK225,4”, the module will enter a standby-stop mode.

There are two ways to return to full power mode:

First way:

- Send any byte on the Rx line

Second way:

- Set FORCE_ON to LOW
- Wait 1sec
- Set FORCE_ON to HIGH.

8.3.2. Reset

In addition, to NMEA command for reset- \$PMTK104*37, external reset is available through $\overline{\text{RESET}}$

pad. Active low signal. Signal logic level of 2.8V.

The module continuously monitors the VCC supply and issue an internal hardware reset if the voltage drops below 2.7 (± 0.1) V. This reset protects the memory from accidental writes during a power down condition. To prevent this, the supply must

be regulated to be within the 2.8-4.3 voltage range, inclusive of load regulation and power supply noise and ripple. Noise and ripple outside of these limits can affect positioning sensitivity and risk tripping the internal voltage supervisors, thereby shutting down the module unexpectedly.

Regulators with good load regulation are recommended in order to prevent power supply glitches as the receiver transitions between power states.

8.3.3. 1PPS

Pulse-Per-Second (PPS) output provides a pulse signal for timing purposes.

The pulse is configurable for required duration, frequency and active high/low via command.

The pulse may vary 30 nS (1 σ). The relationship between the PPS signal and UTC is unspecified.

Use Proprietary MediaTek command PMTK255 to enable or disable this functionality:

- **PMTK255,1 => enable PPS**
- **PMTK255,0 => disable PPS**

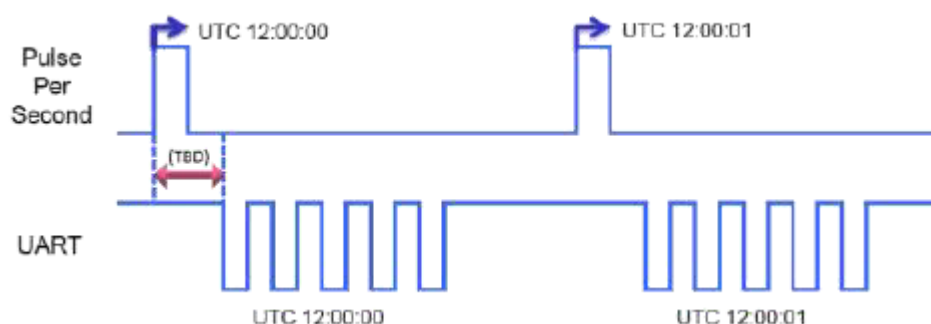


Figure 8. 1PPS AND UTC

1PPS supports 1Hz NMEA output, but at baud rate of 9600 bps, if there are many NMEA sentences

output, per second transmission may exceed one second.

8.3.4. Wakeup

When the ORG4033 is on (full power) the output will be high at 3.3V level.

When the ORG4033 in on Standby or backup mode the output will be low (ground).

Typical output voltage is 3.3V.

On low power modes (Periodic and AlwaysLocate) when the ORG4033 is off the wakeup level is low (and the wakeup returns to high level when the module returns to full power).

9. TYPICAL APPLICATION CIRCUIT

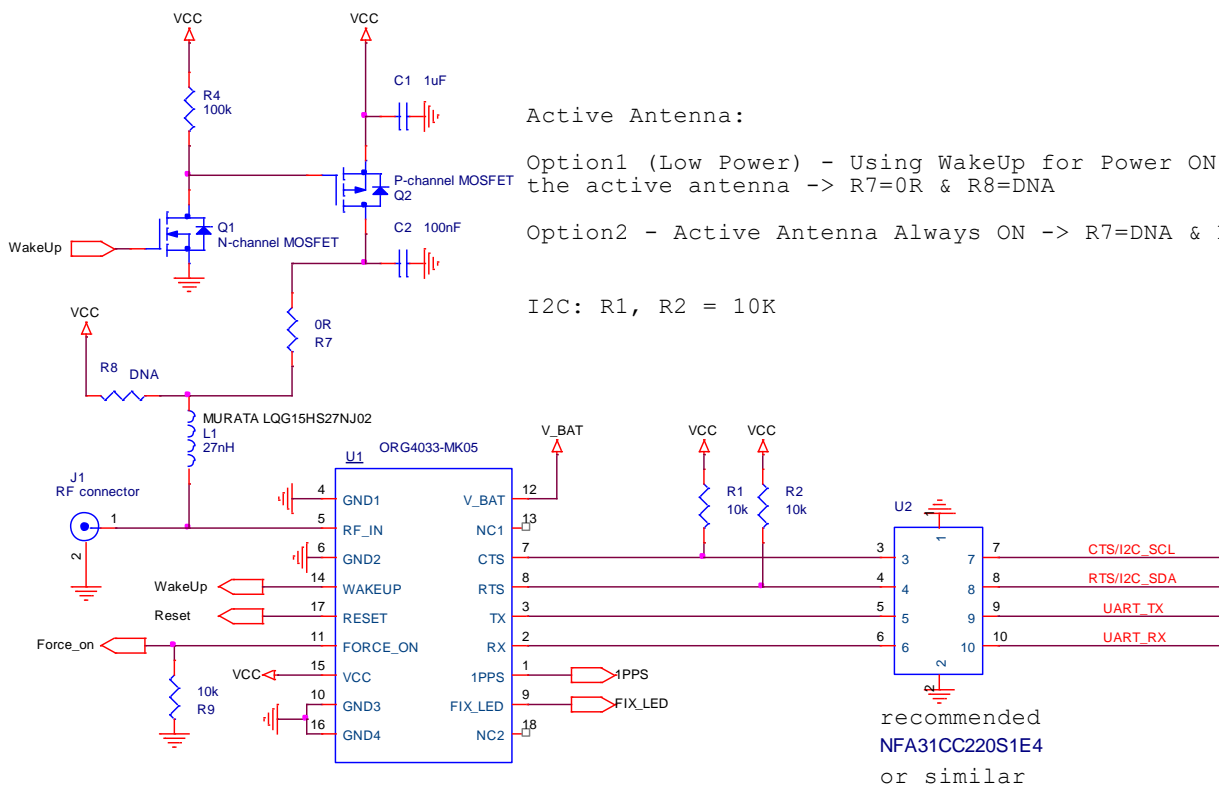


Figure 9. Reference Schematic Diagram



10. RECOMMENDED PCB LAYOUT

10.1. Footprint

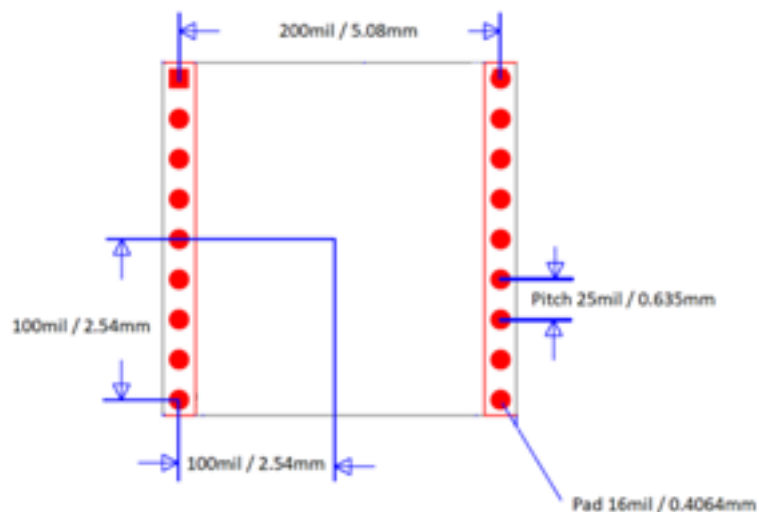


Figure 10. Footprint

10.2. Host PCB

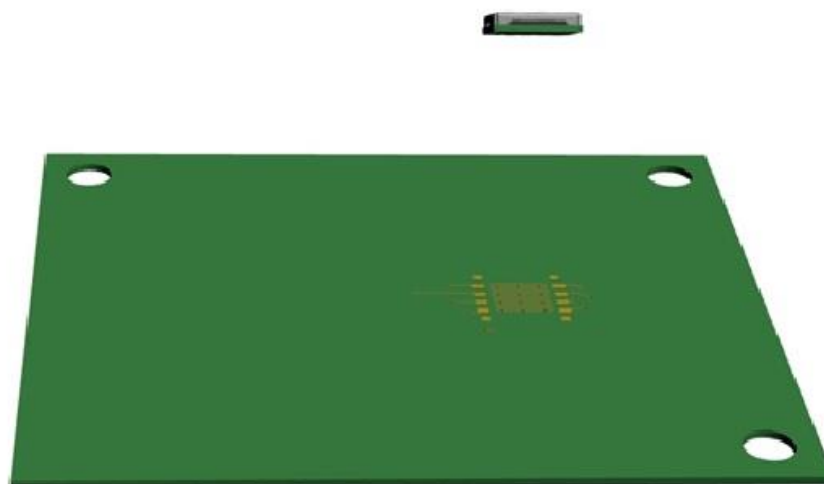


Figure 11. Host PCB

10.3. RF Trace

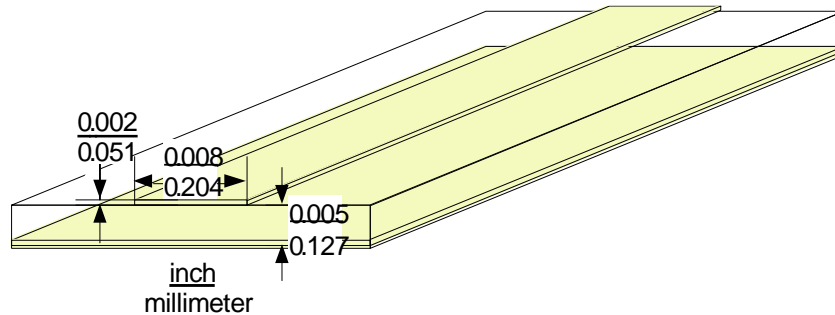


Figure 12. Typical Microstrip PCB Trace On Fr-4 Substrate

10.4. PCB Stack-Up

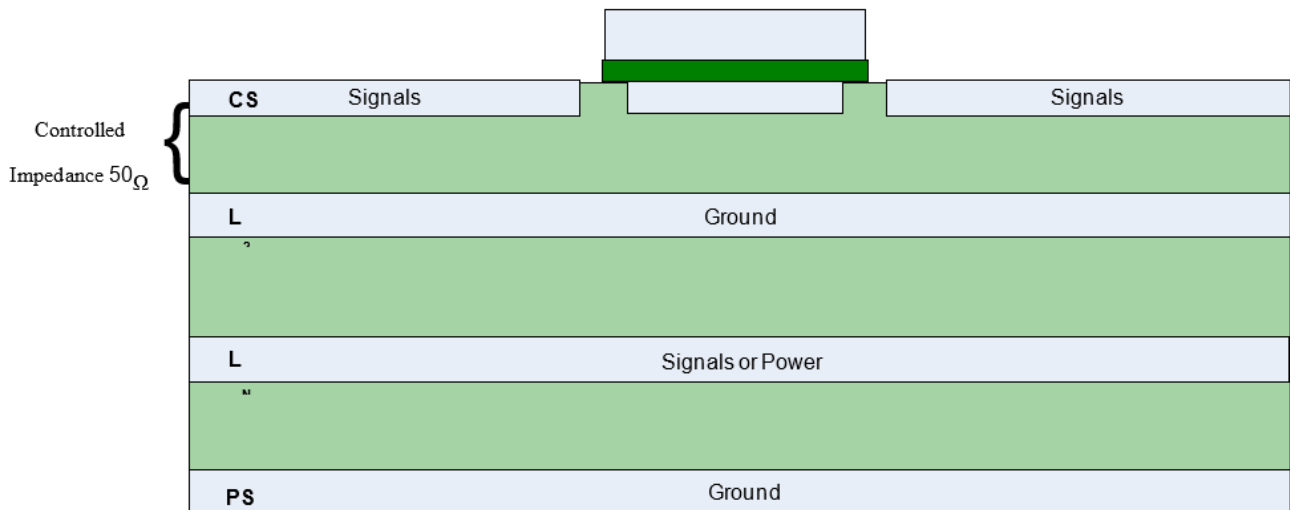


Figure 13. Typical PCB Stack-Up

10.5. PCB Layout Restrictions

Switching and high-speed components, traces and VIAs must be kept away from ORG4033 module.

Signal traces to/from module should have minimum length.

Recommended minimal distance from adjacent active components is 3mm.

Ground pads must be connected to host PCB Ground with shortest possible traces or VIAs.

In case of tight integration constrain or co-location with adjacent high-speed components like CPU or memory, high frequency components like transmitters, clock resonators or oscillators, LCD panels or CMOS image sensors.



11. DESIGN CONSIDERATIONS

This section describes the design considerations of the ORG4033 module.

11.1. Antenna

Antennas for GPS and GLONASS have a wider bandwidth than pure GPS antennas. Some wideband antennas may not have a good axial ratio to block reflections of RHCP GPS and GLONASS signals. These antennas have lower rejection of multipath reflections and tend to degrade the overall performance of the receiver.

11.2. RF

The ORG4033 module operates with received signal levels down to -167dBm and can be affected by high absolute levels of RF signals, moderate levels of RF interference near the GNSS bands and by low-levels of RF noise in GNSS band.

RF interference from nearby electronic circuits or radio transmitters can contain enough energy to desensitize ORG4033. These systems may also produce levels of energy outside of GNSS band, high enough to leak through RF filters and degrade the operation of the radios in ORG4033.

This issue becomes more critical in small products, where there are industrial design constraints. In that environment, transmitters for Wi-Fi, Bluetooth, RFID, cellular and other radios may have antennas physically close to the GNSS receiver antenna.

To prevent degraded performance of ORG4033, OriginGPS recommends performing EMI/jamming susceptibility tests for radiated and conducted noise on prototypes and assessing risks of other factors.



12. COMMANDS DESCRIPTION

Table 13. NMEA Input Commands

Command ID	Description
PMTK000	Test. This command will be echoed back to the sender (for testing the communications link).
PMTK101	Perform a HOT start
PMTK102	Perform a WARM start
PMTK103	Perform a COLD start
PMTK104	Perform a system reset (erasing any stored almanac data) and then a COLD start
PMTK120	Erase aiding data stored in flash memory
PMTK127	Erase EPO data stored in flash memory
PMTK161,0	Standby - Stop mode
PMTK161,1	Standby - Sleep mode
PMTK251,Baudrate	Set NMEA Baudrate
PMTK313,0	Disable SBAS feature
PMTK313,1	Enable SBAS feature
PMTK353,1,0,0,0,0	Enable GPS only mode
PMTK353,0,1,0,0,0	Enable GLO only mode
PMTK353,0,0,0,0,1	Enable BDS only mode
PMTK353,1,1,0,0,0	Enable GPS and GLO mode
PMTK353,1,0,0,0,1	Enable GPS and BDS mode



13. FIRMWARE UPDATES

The FW stored in the internal Flash memory may be upgraded via the serial port TX/RX pads.

In order to update the FW, the following steps should be performed to perform reprogramming:

1. Remove all power to the module.
2. Connect serial port to a PC.
3. Apply main power.
4. Run the software utility to re-flash the module. Clearing the entire flash memory is strongly recommended prior to programming.
5. Upon successful completion of re-flashing, remove main power to the module for a minimum of 10 seconds.
6. Apply main power to the module.
7. Verify the module has returned to the normal operating state.



14. HANDLING INFORMATION

This section describes the handling information of the ORG4033 module.

14.1. Moisture Sensitivity

ORG4033 modules are MSL 3 designated devices according to IPC/JEDEC J-STD-033B standard.

Module in sample or bulk package should be baked prior to assembly at 125°C for 48 hours.

14.2. Assembly

The module supports automatic pick-and-place assembly and reflow soldering processes.

Suggested solder paste stencil is 5 mil to ensure sufficient solder volume.

14.3. Soldering

Reflow soldering of the module always on component side (Top side) of the host PCB according to standard IPC/JEDEC J-STD-020D for LGA SMD.

Avoid exposure of ORG4033 to face-down reflow soldering process.

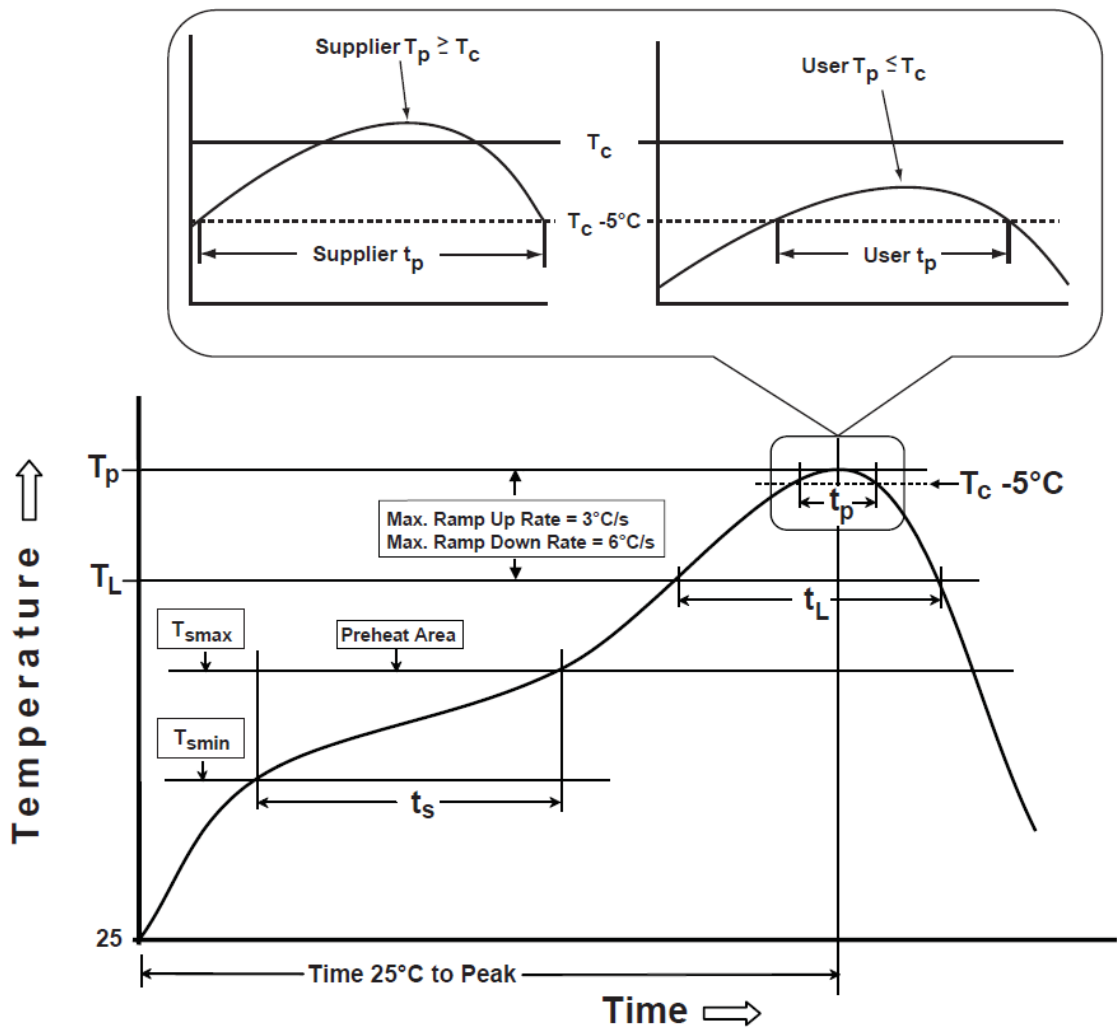


Figure 14. Recommended Soldering Profile

Referred temperature is measured on top surface of the package during the entire soldering process.

Suggested peak reflow temperature is 245°C for 30 sec. for Pb-Free solder paste.

Actual board assembly reflow profile must be developed individually per furnace characteristics.

Reflow furnace settings depend on the number of heating/cooling zones, type of solder paste/flux used, board design, component density and packages used.

Table 14. Soldering Profile Parameters

Symbol	Parameter	Min	Typ	Max	Unit
T _C	Classification Temperature		245		°C
T _P	Package Temperature			245	°C
T _L	Liquidous Temperature		217		°C
T _S	Soak/Preheat Temperature	150		200	°C
t _S	Soak/Preheat Time	60		120	s
t _L	Liquidous Time	60		150	s
t _P	Peak Time		30		s

14.4. Cleaning

If flux cleaning is required, module is capable to withstand standard cleaning process in vapor degreaser with the Solvon® n-Propyl Bromide (NPB) solvent and/or washing in DI water.

Avoid cleaning process in ultrasonic degreaser as specific vibrations may cause performance degradation or destruction of internal circuitry.

14.5. Rework

If localized heating is required to rework or repair the module, precautionary methods are required to avoid exposure to solder reflow temperatures that can result in permanent damage to the device.

14.6. ESD Sensitivity

This product is ESD sensitive device and must be handled with care.



14.7. Safety Information

Improper handling and use can cause permanent damage to the product.

14.8. Disposal Information

This product must not be treated as household waste.

For more detailed information about recycling electronic components contact your local waste management authority.





15. COMPLIANCE

The following standards are applied on the production of ORG4033 modules:

- IPC-6011/6012 Class2 for PCB manufacturing
- IPC-A-600 Class2 for PCB inspection
- IPC-A-610D Class2 for SMT acceptability

ORG4033 modules are manufactured in ISO 9001:2008 accredited facilities.

ORG4033 modules are manufactured in ISO 14001:2004 accredited facilities.

ORG4033 modules are manufactured in OHSAS 18001:2007 accredited facilities.

ORG4033 modules are designed, manufactured and handled in compliance with the Directive 2011/65/EU of the European Parliament and of the Council of June 2011 on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment, referred as RoHS II.



ORG1510 modules are manufactured and handled in compliance with the applicable substance bans as of Annex XVII of Regulation 1907/2006/EC on Registration, Evaluation, Authorization and Restriction of Chemicals including all amendments and candidate list issued by ECHA, referred as REACH.



ORG1510 modules comply with the following EMC standards:

- EU CE EN55022:06+A1(07), Class B
- US FCC 47CFR Part 15:09, Subpart B, Class B
- JAPAN VCCI V-3/2006.04





16. PACKAGING AND DELIVERY

This section describes the packaging and delivery of the ORG4033 module.

16.1. Appearance

ORG4033 modules are delivered in reeled tapes for automatic pick and place assembly process.

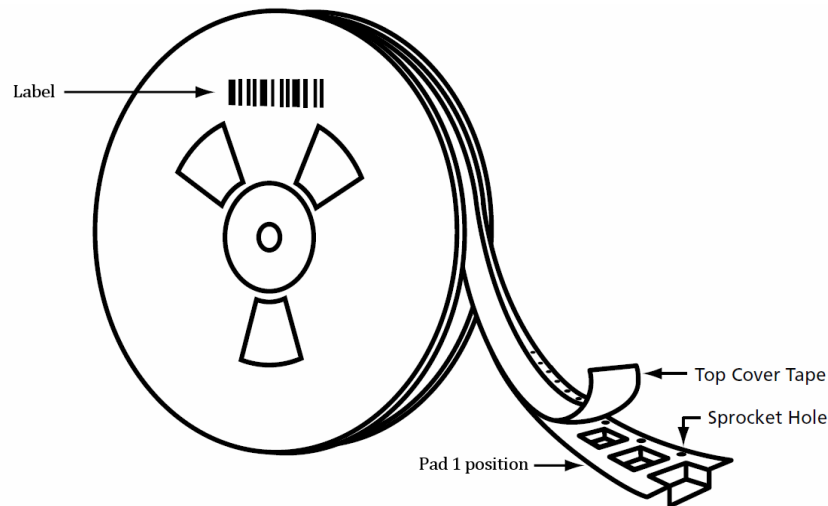


Figure 15. Module Position

ORG4033 modules are packed in 2 different reel types.

Table 15. Reel Quantity

Suffix	TR1	TR2
Quantity	400	1200

Reels are dry packed with humidity indicator card and desiccant bag according to IPC/JEDEC J-STD-033B standard for MSL 3 devices.

Reels are vacuum sealed inside anti-static moisture barrier bags.

Sealed reels are labeled with MSD sticker providing information about:

- MSL
- Shelf life
- Reflow soldering peak temperature
- Seal date

Sealed reels are packed inside cartons.

Reels, reel packs and cartons are labeled with sticker providing information about:

- Description
- Part number
- Lot number
- Customer PO number
- Quantity

- Date code

16.2. Carrier Tape

Carrier tape material - polystyrene with carbon (PS+C).

Cover tape material – polyester based film with heat activated adhesive coating layer.

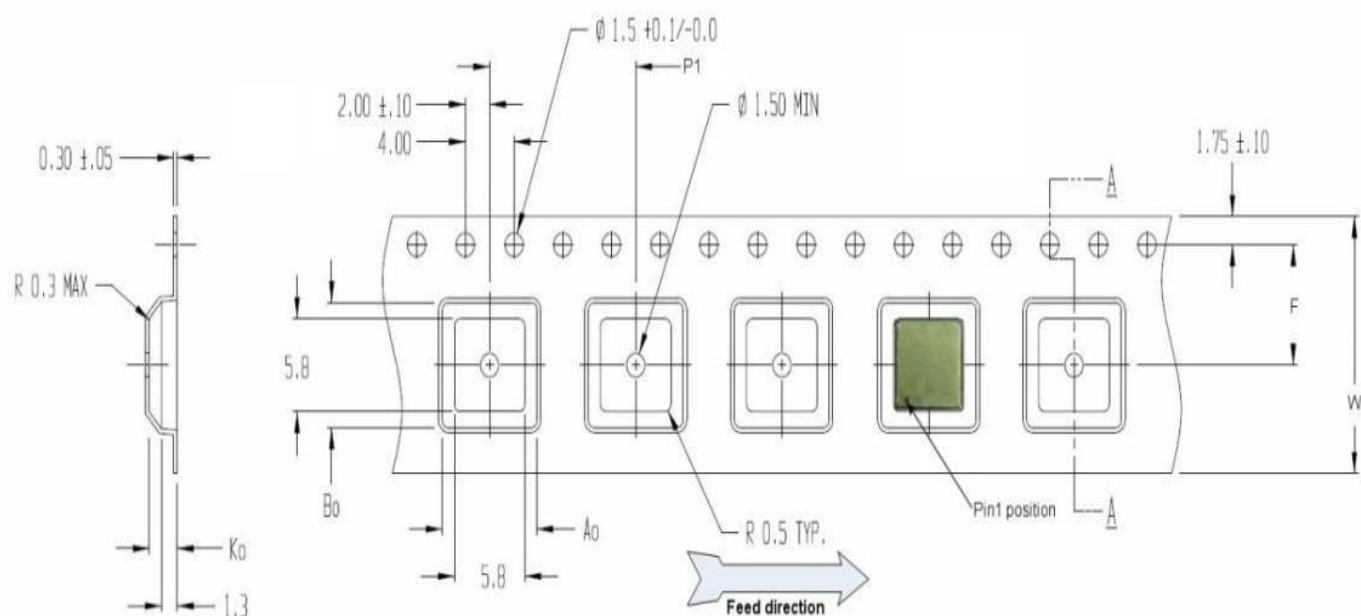


Figure 16. Carrier Tape

Table 16. Carrier Tape Dimensions

	mm	inch
A ₀	6.86 ± 0.1	0.27 ± 0.004
B ₀	6.86 ± 0.1	0.27 ± 0.004
K ₀	3.8 ± 0.1	0.15 ± 0.004
P1	12.0 ± 0.1	0.472 ± 0.004
W	16.0 ± 0.3	0.630 ± 0.012



16.3. Reel

Reel material - antistatic plastic.

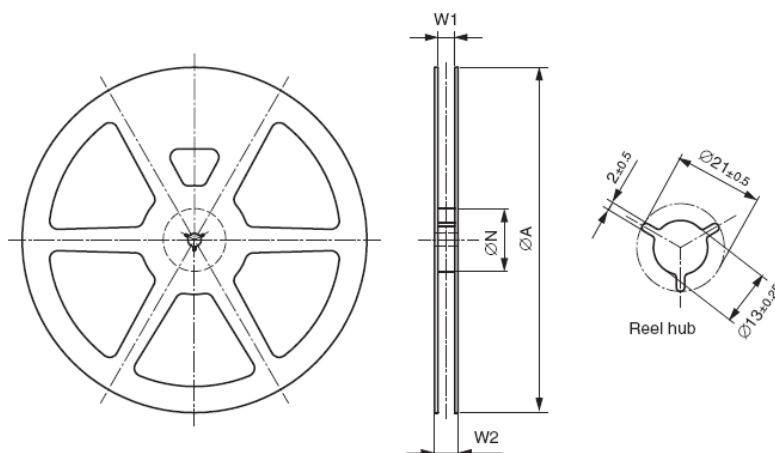


Figure 17. Reel

Table 17. Reel Dimensions

Suffix	TR1		TR2	
	mm	inch	mm	inch
ØA	178.0 ± 1.0	± 0.04	330.0 ± 2.0	13.00 ± 0.08
ØN	60.0 ± 1.0	2.36 ± 0.04	102.0 ± 2.0	4.02 ± 0.08
W1	16.7 ± 0.5	0.66 ± 0.02	16.7 ± 0.5	0.66 ± 0.02
W2	19.8 ± 0.5	0.78 ± 0.02	22.2 ± 0.5	0.87 ± 0.02

17. ORDERING INFORMATION

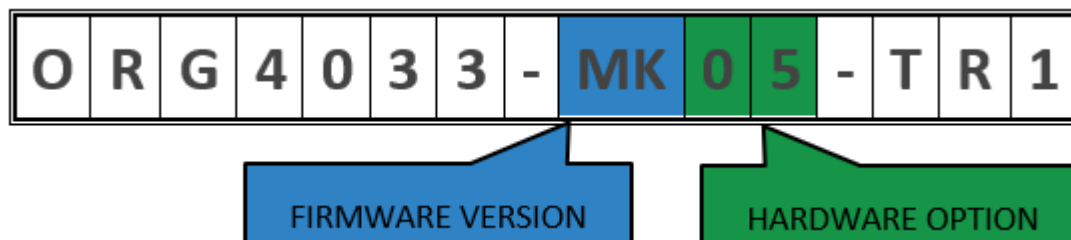


Figure 18. Ordering Options

Table 18. Orderable Devices

Part Number	FW Version	HW Option	V _{CC} Range	Packaging	SPQ
ORG4033-MK05-TR1	MK	05	3.3V	REELED TAPE	400
ORG4033-MK05-TR2	MK	05	3.3V	REELED TAPE	1200
ORG4033-MK05-TR1-SPI	MK	05	3.3V	REELED TAPE	400
ORG4033-MK05-TR2-SPI	MK	05	3.3V	REELED TAPE	1200
ORG4033-MK05-UAR	MK	05	5V USB	EVALUATION KIT	1
ORG4033-MK05-UAR-SPI	MK	05	5V USB	EVALUATION KIT	1

Appendix A. The ORG4033-MK05 Module

The ORG4033-MK05 version has an option to connect a coin battery (for example ECR2025 coin battery) to provide power in backup mode. Minimum voltage that the backup battery will support is 2.8V.

With a battery connection, after waking up, the receiver uses:

1. All internal aiding, including RTC time, Ephemeris, and Last Position, resulting in the fastest possible TTFF in either hot or warm start modes.
2. Configuration settings stored in flash after turning power off.

To keep alive the RTC time, the following circuit implementation using a 3V coin battery, can be used.

In addition, you should use a charger for the battery or separating the VCC and V_BACKUP with using controlled LDO for each of them.

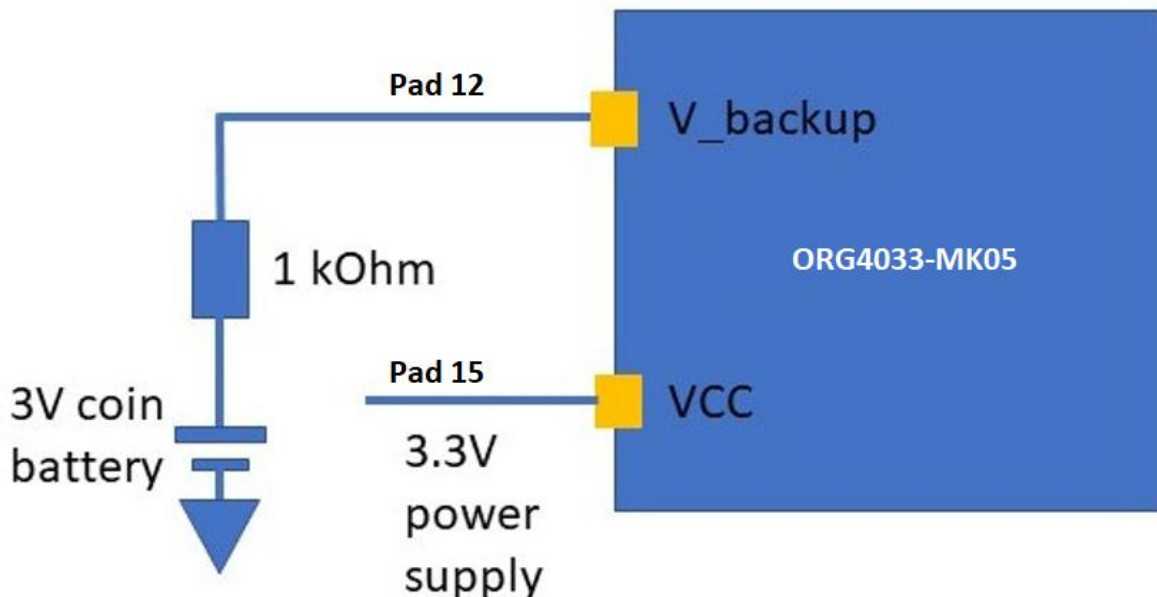


Figure 19. Battery Backup Implementation

If a battery is not connected to pad 12 in ORG4033-MK05, connection between pads 12 and 15 is a MUST in order to operate the module.